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(71) Applicant: FUJITSU LIMITED
Kawasaki-shi, Kanagawa 211-8588 (JP)

(72) Inventors:
- Asao, Shigeharu
Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Koizumi, Haruo
Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)
- Kanazawa, Yoshikazu
Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP)

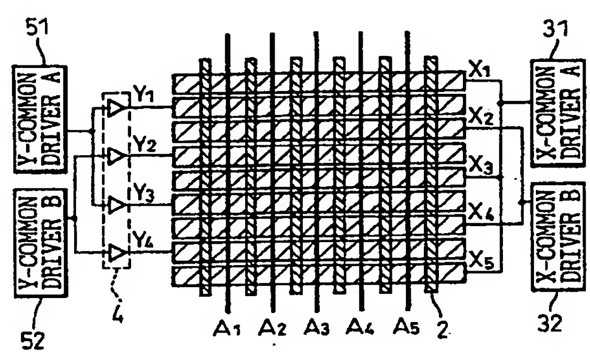
(74) Representative:
Fenlon, Christine Lesley et al
Haseltine Lake & Co.,
Imperial House,
15-19 Kingsway
London WC2B 6UD (GB)

(54) Plasma display panel

(57) A method of driving a plasma display panel, the method comprising:

a reset period in which a reset discharge is carried out in a plurality of discharge cells by applying prescribed voltages to the sustain electrodes X_i, scan electrodes Y_n, and address electrodes A_j to accomplish a uniform charge distribution among the plurality of discharge cells;
an address period in which a write discharge is carried out in selected discharge cells between the scan electrodes Y_n and the address electrodes A_j, thereby performing selective writing that matches display data; and
a sustain discharge period in which sustain discharge pulses are applied between the sustain electrodes X_i and the scan electrodes Y_n, thereby causing a discharge glow for the display at the discharge cells in which the writing has been performed in the address period, wherein potential differences between the odd-numbered sustain electrodes X_{2i-1} and the even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and the odd-numbered scan electrodes Y_{2n-1} during the reset period of an odd field in which a display is produced between the odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, and potential differences between the odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between the even-numbererd sustain electrodes X_{2i} and scan electrodes Y_{2n} during the reset period of an even field in which a display is produced between the odd-numbered sustain electrodes X_{2i-1} and even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, are each held below a discharge initiating voltage between the respective electrodes.

Fig.10



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Description

The present invention relates to a plasma display panel of the kind which comprises discharge cells having a memory effect and to a method of driving a plasma display panel of this kind.

An AC (alternating current) plasma display panel (PDP) operates by light emission via a sustaining discharge formed by applying voltage pulses alternately to a pair of sustain electrodes. The discharge itself forms in one to several microseconds after application of the voltage pulse, but positively charged ions generated as a result of the discharge are accumulated on the surface of an insulating layer overlying the electrode supplied with a negative voltage. At the same time, electrons, i.e. negative charges, are generated and accumulate on the surface of an insulating layer overlying the electrode supplied with a positive voltage. These accumulated positive and negative charges are called wall charges.

Once the wall charges have been formed after creating a discharge with the application of a high voltage pulse (write pulse), the threshold voltage required to cause a subsequent discharge is lowered so that applying a voltage pulse (sustain discharge pulse) lower in voltage than the initial voltage is sufficient to generate a discharge, as this sustain discharge voltage is superimposed on the voltage provided by the accumulated wall charges. That is, the AC PDP has the characteristic that a discharge cell, once subjected to a write pulse with the resulting formation of a wall charge, can be maintained in the discharging state by applying lower voltage sustain discharge pulses alternately in reverse polarity. This is called the memory effect or memory capability. Generally, AC PDPs display images use this memory effect.

Figures 10 to Figure 13b of the accompanying drawings show an interlaced plasma display panel and a method of driving the same according to Japanese Patent Application No. 8-194320.

Figure 10 of the accompanying drawings is a plan view showing an interlaced PDP. Scan electrodes Y_n and sustain electrodes X_i, extending in parallel to each other, are paired in adjacent positions, each pair forming one display line. Address electrodes A_j are arranged intersecting at right angles with the scan electrodes Y_n and sustain electrodes X_i, a discharge cell being formed in each intersection region. For simplicity, four scan electrodes Y_1 to Y_4, five sustain electrodes X_1 to X_5, and five address electrodes A_1 to A_5 are shown in the figure, but actually, a large number of such electrodes are provided according to the required display resolution. Each discharge cell is spatially decoupled from horizontally adjacent discharge cells by barriers 2 (also called ribs).

Of the sustain electrodes X_i, the odd-numbered electrodes are connected to an X-common driver A and the even-numbered electrodes are connected to an X-common driver B. The X-common driver A is indicated by reference numeral 31 and the X-common driver B by reference numeral 32. The X-common drivers A and B supply pulses, such as a blanket write pulse for a reset discharge and a sustain discharge pulse (Vs), to the sustain electrodes X_i. The scan electrodes Y_n are individually connected to Y-scan drivers 4 and are independently driven by respective ones of the Y-scan drivers 4. Of the scan electrodes Y_n, the odd-numbered electrodes Y_{2n-1} are connected to a Y-common driver A and the even-numbered electrodes Y_{2n} are connected to a Y-common driver B. The Y-common driver A is indicated by reference numeral 51 and the Y-common driver B by reference numeral 52. When performing a write discharge in accordance with an input signal, scan pulses (-Vy) to be applied to the respective scan electrodes Y_n are supplied from respective ones of the Y-scan drivers 4. When performing a sustain discharge for display based on the write discharge, sustain pulses (Vs) to be applied to the respective scan electrodes Y_n are supplied from the Y-common drivers A and B to the scan electrodes Y_n via the respective Y-scan drivers 4. The address electrodes A_j are individually connected to address drivers (not shown) and are independently driven by the respective address drivers.

In the above-described interlaced driving method, the discharge is carried out by utilizing slits (electrode gaps) located on both sides of each of the scan electrodes Y_n. This differs from earlier, conventional three-electrode, surface-discharge PDPs, in which the slits used for discharging are predetermined at the beginning, such as the slits between Y_1 and X_1, between Y_2 and X_2, and so on. As a result, to obtain N display lines, a total of N x 2 electrodes, namely the scan electrodes Y_n and the sustain electrodes X_i, are required. This impedes the realization of high-resolution panels. Whereas, with the above interlaced method of JP 8-194320, by dividing the X-common driver into two sections A and B, it is possible to supply different signals to the sustain electrodes X_i and X_{i+1} located adjacently on both sides of each scan electrode Y_n to which the scan signal is supplied.

When performing discharging in accordance with a video signal, a discharge is caused between the scan electrode Y_n and address electrode A_j by an address signal supplied to the address electrode in synchronism with the scan signal, and using this discharge as a trigger, a discharge is also caused between the scan electrode Y_n and a sustain electrode X_i adjacent thereto, thereby accomplishing the writing. In the interlaced method, one or the other of the two sustain electrodes X_i and X_{i+1} adjacent to the scan electrode Y_n can be selected for the discharge to be caused between the scan electrode Y_n and the selected sustain electrode X_i or X_{i+1}. That is, with the above method, all the slits can be used for discharging, which means that a total of N+1 electrodes, the scan electrodes Y_n and sustain electrodes X_i combined, are required to obtain N display

lines. In other words, in comparison with earlier, conventional three-electrode, surface-discharge PDPs, the number of display lines can be almost doubled with a given number of electrodes.

Figure 11 of the accompanying drawings is a cross-sectional view showing the above-described interlaced PDP. A discharge space 13 is formed between back and front glass substrates 11 and 14 respectively disposed opposite to each other. Scan electrodes Y_n and sustain electrodes X_i, extending parallel to each other, are formed on a front glass substrate 14, each of these electrodes consisting of a transparent electrode 15 and a bus electrode 16. The transparent electrode 15 is formed from indium tin oxide (ITO) or the like and transmits light reflected from a phosphor not shown. The bus electrode 16 is formed on top of the transparent electrode 15 in order to prevent a voltage drop due to the transparent electrode 15, which has a relatively large resistance compared to an ordinary wiring metal. Since it is opaque, the bus electrode 16 must be formed as a thin line so as not to reduce the display area. These electrodes are covered with a dielectric layer 17.

The back glass substrate 11 is disposed opposite to the front glass substrate 14 and has formed on it address electrodes A_j which, in plan view, cross the scan electrodes Y_n and the sustain electrodes X_i at right angles . Like the scan electrodes Y_n and sustain electrodes X_i, the address electrodes A_j are covered with a dielectric layer 12. Though not shown here, phosphors having red, green and blue light emitting properties are formed covering the address electrodes.

In earlier, conventional PDPs, since the slits used for discharging are predetermined, the bus electrode 16 is often formed on one edge of the transparent electrode 15. In the above interlaced PDP, on the other hand, since the slits used for discharging are not predetermined, the bus electrode 16 is disposed approximately in the centre of the transparent electrode 15. References L1 to L3 are used to indicate the slits. In the figure, the discharge is shown as occurring in the slits L1 and L3, but at the next timing, the discharge occurs in the slit L2. In this way, selective discharging is carried out on all the slits.

Figure 12 of the accompanying drawings shows a frame structure according to the interlaced method, illustrating one image display frame in the above interlaced PDP. This structure is disclosed in the aforementioned Japanese Patent Application No. 8-194320. The frame structure is based on the ADS Subfield Method of Japanese Patent Application No. 5-310937 wherein an address period (A), during which a write discharge is carried out in accordance with display data, and a sustain period (S), during which a sustain discharge (display) is carried out based on the written data, are separated in time and a gradation display is produced by combining a plurality of differently weighted subfields. In practice, a reset period (R) for initialization is placed before the address period.

One frame is divided into an odd field and an even field, each field consisting of a plurality of subfields (in the illustrated example, the first to the third subfield). In the odd field, for example, the slits L1 and L3 in Figure 10 of the accompanying drawings are used to produce the display, while in the even field the slit L2 is used. In the subfields, the sustain periods are T1, 2T1, and 4T1, respectively and the sustain discharge is carried out a number of times that is substantially proportional to the length of the period. By selecting the subfields as desired, a display with 8 grey scale levels can be achieved. In like manner, if the number of subfields is set to 8 and the ratio among the sustain periods is chosen to be 1:2:4:8:16:32:64:128, a display with 256 grey scale levels can be achieved. Here, the sustain period ratios need not necessarily be set according to a geometric progression. Instead, more than one subfield may be set with the same number of sustain discharges, or the number of discharges may be adjusted according to the actual display brightness.

Figures 13a and 13b of the accompanying drawings show waveform diagrams of the interlaced driving. As stated above, one frame is divided into two portions, an odd field and an even field, each of which is further divided into a plurality of subfields. In the figures, only one subfield is shown from each of the odd and even fields. Each subfield consists of a reset period, an address period and a sustain period. The reset period is for resetting the wall charges remaining from the immediately preceding subfield, the address period is for performing a write discharge according to display data and thereby accumulating wall charges within designated discharge cells and the sustain period is for performing a sustain discharge to produce a display in the discharge cells where the wall charges have been accumulated during the address period.

First, the driving for the odd field will be described. In the reset period, a blanket write pulse Vs+Vw is applied to all the sustain electrodes X_i. Since all the scan electrodes are held at ground potential, the potential difference Vs+Vw between the sustain electrodes X_i and scan electrodes Y_n exceeds the discharge initiating voltage between the electrodes, accomplishing the reset discharge between all the electrodes, i.e. in all the slits. At this time, a pulse Vaw is applied to the address electrodes A_j to reduce the potential difference with respect to the sustain electrodes Xi in order to prevent a discharge from occurring between them. As a result of the blanket write discharge in all of the slits, excessive wall charges of different polarities are accumulated on the respective electrodes. When all the electrodes are brought to the same potential (in this case, ground potential) after applying the write pulse, the potential difference of the wall charge itself exceeds the discharge initiating voltage and a self-erase discharge occurs, which neutralizes and erases the wall charge on each electrode.

The address period is further divided into the first

half and second half portions. In the first half portion, for example, the odd-numbered scan electrodes Y_{2n-1} are scanned in sequence. In the second half portion, the even-numbered scan electrodes are scanned in sequence. In the first half portion, a scan pulse -Vy is applied in sequence to the scan electrodes Y_{2n-1}. This scan pulse -Vy is applied in such a manner as to be superimposed on a base pulse -Vsc which is maintained throughout the address period. In synchronism with the scan pulse -Vy, an address pulse (data) Va is selectively applied to the address electrodes A_j, thereby accomplishing the write discharge between the scan electrodes Y_{2n-1} and the selected address electrodes A_j. At this time, of the sustain electrodes X_i, only the odd-numbered electrodes X_{2i-1} are held at potential Vx throughout the first half period. This makes it possible to specify slits for discharging. That is, the discharge fired by the write discharge occurs only between the scan electrodes Y_{2n-1} and the sustain electrodes X_{2i-1} supplied with the pulse Vx, and wall charges are accumulated in the discharge cells formed by the scan electrodes Y_{2n-1} and the sustain electrodes X_{2i-1}.

Next, in the second half portion of the address period, the remaining even-numbered scan electrodes Y_{2n} are scanned in sequence, in synchronism with which the address pulse Va is selectively applied to the address electrodes A_j. At the same time, the pulse Vx is applied only to the even-numbered sustain electrodes X_{2i}, as a result of which the discharge is selectively caused between the scan electrodes Y_{2n} and the sustain electrodes X_{2i}, and wall charges are accumulated.

In the sustain period, by applying the sustain discharge pulse Vs alternately to the scan electrodes Yn and the sustain electrodes Xi, the sustain discharge for display is carried out on the discharge cells where the wall charges have been accumulated during the address period. At this time, in the odd field, the odd-numbered scan electrodes Y_{2n-1} and the even-numbered sustain electrodes X_{2i}, and the even-numbered scan electrodes Y_{2n} and the odd-numbered sustain electrodes X_{2i-1}, are respectively maintained in phase, so that a potential difference does not occur in the slits between the respective electrodes and the sustain discharge does not take place in these slits. In this way, in the odd field, the sustain discharge takes place only between the odd-numbered electrodes and between the even-numbered electrodes.

The driving for the subsequent even field will be described next.

In the reset period, the same operation as in the first described odd field is performed, likewise accomplishing the reset discharge in all the slits which is followed by the self-erase discharge.

In the address period, in the first half portion, the odd-numbered scan electrodes Y_{2n-1} are likewise scanned in sequence, but, at this time, of the sustain electrodes X_i, the even-numbered sustain electrodes X_{2i} are held at the potential Vx. As a result, in the even field, the discharge fired by the write discharge occurs only between the odd-numbered scan electrodes Y_{2n-1} and even-numbered sustain electrodes X_{2i}, and wall charges are accumulated in the discharge cells formed by the scan electrodes Y_{2n-1} and the sustain electrodes X_{2i}.

Next, in the second half portion of the address period, the remaining even-numbered scan electrodes Y_{2n} are scanned in sequence and, at the same time, the pulse Vx is applied only to the odd-numbered sustain electrodes X_{2i-1}, as a result of which the discharge is selectively caused between the scan electrodes Y_{2n} and the sustain electrodes X_{2i-1} and wall charges are accumulated.

In the sustain period that follows, the odd-numbered electrodes and the even-numbered electrodes are respectively maintained in phase, so that a potential difference is not produced in the slits between the respective electrodes, and a sustain discharge is not generated in these slits. In this way, in the even field, sustain discharge takes place only between the odd-numbered electrodes and even-numbered electrodes.

The above driving method, however, has the undesirable property that contrast is decreased owing to the reset discharge.

A general criticism that has been levelled against PDPs is their low contrast compared with cathode ray tubes and some other display devices. One of the causes for the relatively low contrast in known PDPs is the unwanted light emission caused by the reset discharge. More specifically, in a PDP, the light emission that directly contributes to the display of an image is that caused by the sustain discharge, but discharging during other periods also produces light emission. It has therefore been pointed out that the unwanted light emission by the reset discharge, that does not directly contribute to the display of an image, contributes to reducing the black level during non-display periods.

It has been confirmed by experiments conducted by the present inventors that when the interlaced method is employed, the contrast tends to further decrease. The cause has been discovered to be the discharge that occurs in all the slits during the reset period. That is, in the odd field, the slits between the odd-numbered electrodes and the slits between the even-numbered electrodes are actually subjected to sustain discharge, but the reset discharge is also performed on the remaining slits. Likewise, in the even field, the slits between the odd-numbered electrodes and even-numbered electrodes are actually subjected to sustain discharge, but the reset discharge is also performed on the remaining slits. As a result, in the interlaced method, the reset discharge is performed twice on each slit, once each in the odd field and in the even field. In non-interlaced PDPs, reset discharge is performed once on each line in one subfield. Therefore, by simple comparison, the number of reset discharges is doubled. This is a serious problem faced by the interlaced method, which is intended

for high-resolution displays.

According to a first aspect of the present invention, there is provided a method of driving a plasma display panel in which a plurality of sustain electrodes X_i and a plurality of scan electrodes Y_n are arranged parallel to each other on a first substrate in a corresponding relationship to an equal number of display lines, and a plurality of address electrodes A_j electrically isolated from the sustain electrodes X_i and the scan electrodes Y_n are arranged on a second substrate, opposing the first substrate, in such a manner as to intersect with the sustain electrodes X_i and scan electrodes Y_n (as viewed in the viewing direction of the plasma display panel) to form discharge cells at the intersection regions, the method comprising: an odd field in which a display is produced between odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, and an even field in which a display is produced between the odd-numbered sustain electrodes X_{2i-1} and even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, each of the odd and even fields including: a reset period in which a reset discharge is carried out in a plurality of discharge cells by applying prescribed voltages to the sustain electrodes X_i, scan electrodes Y_n, and address electrodes A_j to accomplish a uniform charge distribution among the plurality of discharge cells; an address period in which a write discharge is carried out in selected discharge cells between the scan electrodes Y_n and the address electrodes A_j, thereby performing selective writing that matches display data; and a sustain discharge period in which sustain discharge pulses are applied between the sustain electrodes X_i and the scan electrodes Y_n, thereby causing a discharge glow for the display at the discharge cells in which the writing has been performed in the address period, wherein potential differences between the odd-numbered sustain electrodes X_{2i-1} and the even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and the odd-numbered scan electrodes Y_{2n-1} during the reset period of the odd field, and potential differences between the odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between the even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} during the reset period of the even field, are each held below a discharge initiating voltage between the respective electrodes.

In the method of the first aspect, during the reset period of each of the odd and even fields, the voltage applied to the slits that are not contributing to the display of an image, that is, the slits where the sustain discharge is not carried out, is held below the discharge initiating voltage. As a result, the reset discharge occurs only in the slits that are contributing to the display, and no reset discharge occurs in the slits that are not contributing to the display. This serves to reduce the unwanted discharge that does not contribute to the display, and a contrast drop can thus be prevented.

According to a second aspect of the present invention, there is provided a plasma display panel in which a plurality of sustain electrodes X_i and a plurality of scan electrodes Y_n are arranged parallel to each other on a first substrate in corresponding relationship to an equal number of display lines, and a plurality of address electrodes A_j electrically isolated from the sustain electrodes X_i and scan electrodes Y_n are arranged on a second substrate, opposing the first substrate, in such a manner as to intersect with the sustain electrodes X_i and scan electrodes Y_n (as viewed in the viewing direction of the plasma display panel) to form discharge cells in the intersection regions, the plasma display panel comprising: an odd field in which a display is produced between odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, and an even field in which a display is produced between the odd-numbered sustain electrodes X_{2i-1} and even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, each of the odd and even fields including: a reset period in which a reset discharge is carried out in a plurality of discharge cells by applying prescribed voltages to the sustain electrodes X_i, the scan electrodes Y_n, and the address electrodes A_j to accomplish a uniform charge distribution among the plurality of discharge cells; an address period in which a write discharge is carried out in selected discharge cells between the scan electrodes Y_n and the address electrodes A_j, thereby performing selective writing that matches display data; and a sustain discharge period in which sustain discharge pulses are applied between the sustain electrodes X_i and the scan electrodes Y_n, thereby causing a discharge glow for the display at the discharge cells in which the writing has been performed in the address period, wherein potential differences between the odd-numbered sustain electrodes X_{2i-1} and the even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and the odd-numbered scan electrodes Y_{2n-1} during the reset period of the odd field, and potential differences between the odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between the even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} during the reset period of the even field, are each held below a discharge initiating voltage between the respective electrodes.

According to a third aspect of the present invention, there is provided a display apparatus comprising: a plasma display panel in which a plurality of sustain electrodes X_i and a plurality of scan electrodes Y_n are arranged parallel to each other on a first substrate in a relationship corresponding to an equal number of display lines, and a plurality of address electrodes A_j electrically isolated from the sustain electrodes X_i and scan

electrodes Y_n are arranged on a second substrate, opposing the first substrate, in such a manner as to intersect with the sustain electrodes X_i and scan electrodes Y_n (as viewed in the viewing direction of the plasma display panel) to form discharge cells at the intersection regions; and drive circuits for respectively driving the sustain electrodes X_i, scan electrodes Y_n, and address electrodes A_j, wherein there are provided an odd field in which a display is produced between odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, and an even field in which a display is produced between the odd-numbered sustain electrodes X_{2i-1} and even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, each of the odd and even fields including: a reset period in which a reset discharge is carried out in a plurality of discharge cells by applying prescribed voltages to the sustain electrodes X_i, scan electrodes Y_n, and address electrodes A_j to accomplish a uniform charge distribution among the plurality of discharge cells; an address period in which a write discharge is carried out in selected discharge cells between the scan electrodes Y_n and the address electrodes A_j, thereby performing selective writing that matches display data; and a sustain discharge period in which sustain discharge pulses are applied between the sustain electrodes X_i and the scan electrodes Y_n, thereby causing a discharge glow for the display at the discharge cells in which the writing has been performed in the address period, wherein potential differences between the odd-numbered sustain electrodes X_{2i-1} and the even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and the odd-numbered scan electrodes X_{2n-1} during the reset period of the odd field, and potential differences between the odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between the even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} during the reset period of the even field, are each held below a discharge initiating voltage between the respective electrodes.

With the teachings of the present invention it is thus possible to provide an interlaced plasma display panel and a method for driving the same in which the contrast drop inherent in the above-described previously contemplated interlaced plasma display panels is avoided.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:-

Figures 1a and 1b are waveform diagrams illustrating a first embodiment of the present invention;
Figures 2a and 2b are waveform diagrams illustrating a second embodiment of the present invention;
Figures 3a and 3b are waveform diagrams illustrating a third embodiment of the present invention;
Figures 4a and 4b are waveform diagrams illustrating a fourth embodiment of the present invention;
Figures 5a and 5b are waveform diagrams illustrating a fifth embodiment of the present invention;
Figures 6a and 6b are waveform diagrams illustrating a sixth embodiment of the present invention;
Figures 7a and 7b are waveform diagrams illustrating a seventh embodiment of the present invention;
Figure 8 is a circuit diagram showing an X-side driver embodying the present invention;
Figure 9 is a circuit diagram showing Y-side drivers embodying the present invention;
Figure 10 is a plan view showing an interlaced plasma display panel;
Figure 11 is a cross-sectional view showing the interlaced plasma display panel of Figure 10;
Figure 12 is a diagram showing a frame structure according to an interlaced method; and
Figures 13a and 13b show waveform diagrams of the interlaced driving of an interlaced plasma display panel.

Figures 1a and 1b are waveform diagrams illustrating a first embodiment of the present invention; shown here are waveforms in one frame which consists of an odd field and an even field. In fact, the odd and even fields each consist of a plurality of subfields having different sustain period lengths, as shown in Figure 12, but for simplicity, only one subfield is shown here for each field.

As shown, each subfield consists of a reset period, an address period, and a sustain period. When the preceding subfield is completed, wall charges corresponding to the display in that subfield remain, so that a reset discharge is carried out in the reset period at the beginning of the next subfield. This discharge is a strong discharge caused by applying between sustain electrodes Xi and scan electrodes Y_n a voltage exceeding the discharge initiating voltage between the electrodes, and is carried out to even out the charge distribution among discharge cells, regardless of the discharge state in the immediately preceding subfield. In the embodiments of the present invention, each electrode potential at the time of reset discharge is set so that for display slits the potential difference between electrodes becomes larger than the discharge initiating voltage, and for non-display slits the potential difference between electrodes becomes smaller than the discharge initiating voltage.

The driving in the odd field according to the present embodiment will be described first. In the odd field, a pulse Vs of positive polarity is applied to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} (i is a natural number), and a pulse -Vw of negative polarity is applied to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} in is a natural number). At the same time, the negative polarity pulse -Vw is applied to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}, and the positive polarity pulse Vs is applied to the even-numbered scan elec-

trodes Y_2, Y_4, ..., Y_{2n}. As a result, the potential difference between the odd-numbered sustain electrodes and scan electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, and that between the even-numbered sustain electrodes and scan electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, which form the display slits in the odd field, become Vs+Vw. With Vs+Vw set equal to or larger than the discharge initiating voltage between the electrodes, the reset discharge is carried out in each display slit. On the other hand, the potential difference between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, and that between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., X_{2n}-Y_{2i-1}, which form the non-display slits in the odd field, are both equal to zero, so that discharge does not occur between them. In this way, in the present embodiment, the reset discharge is carried out only for the display slits.

(n.b. In the previously contemplated designs, the pulse Vaw is applied to the address electrodes at the same time as the application of the blanket write pulse, but this is not necessary in the present embodiment, because the voltage applied to the sustain electrodes X_i and scan electrodes Y_n is lower than the corresponding voltage in the previously contemplated designs and, therefore, there is no possibility of causing a discharge between these electrodes and the address electrodes).

As a result of the reset discharge, excessive wall charges of opposite polarities are accumulated on both electrodes. Therefore, by making the potentials of both electrodes equal, and preferably by bringing them to ground potential, a self-erase discharge occurs to the wall charges which are thus neutralized.

In the address period that follows, a write discharge that matches input data (video data) is carried out. Here, we adopted the method in which writing to the odd-numbered electrodes is performed first, and then writing to the even-numbered electrodes is performed. More specifically, the scan pulse -Vy is applied in sequence to the odd-numbered scan electrodes, Y_1, Y_3, ..., Y_{2n-1}. Since the base pulse -Vsc is applied to each scan electrode Y_n throughout the address period, the scan pulse -Vy is superimposed on the base pulse -Vsc. Data pulse Va is selectively applied to the address electrodes A_j in accordance with the input signal, so that the discharge takes place between the selected address electrodes and the scan electrodes Y_{2n-1} supplied with the scan pulse -Vy. At this time, in the odd field, since the pulse Vx is applied only to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}, the write discharge is carried out only between the odd-numbered sustain electrodes and scan electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, and wall charges are thus accumulated on both electrodes. Next, the scan pulse -Vy is applied in sequence to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n}. Here again, since the data pulse Va is selectively applied to the address electrodes A_j, and the pulse Vx is now applied only to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}, the write discharge is carried out only between the even-numbered sustain electrodes and scan electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, and wall charges are thus accumulated on both electrodes.

In the sustain period that follows, a sustain discharge pulse Vs is applied alternately to the sustain electrodes X_i and scan electrodes Y_n that form the display slits, thus carrying out a sustain discharge in the discharge cells in which the write discharge has been carried out. At this time, to prevent a discharge from occurring between the sustain electrodes X_i and scan electrodes Y_n that form the non-display slits, a voltage pulse of the same phase is applied to the sustain electrodes X_i and scan electrodes Y_n that form the non-display slits. More specifically, in the odd field, the sustain discharge pulse is applied alternately between the odd-numbered sustain electrodes and scan electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, and- also between the even-numbered sustain electrodes and scan electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, which form the display slits, but this pulse is in phase between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, and also between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., X_{2n}-Y_{2i-1}, which form the non-display slits.

Next, in the even field, the display slits are now located between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, and also between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., X_{2n}-Y_{2i-1}. The applied voltage to each display slit is the same as that in the odd field. More specifically, in the even field, the positive polarity pulse Vs is applied to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} and the negative polarity pulse -Vw to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}. At the same time, the negative polarity pulse -Vw is applied to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n} and the positive polarity pulse Vs to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}. As a result, the potential difference between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, and that between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., Y_{2n}-Y_{2i-1}, which form the display slits in the odd field, become Vs+Vw exceeding the discharge initiating voltage between the electrodes, and the reset discharge is thus carried out in each display slit. On the other hand, the potential difference between the odd-numbered sustain electrodes and scan electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, and that between the even-numbered sustain electrodes and scan electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, which form the non-display slits in the even field, are both equal to zero, so that discharge does not occur between them. In this way, the reset dis-

charge is carried out only for the display slits. After completion of the reset discharge, a self-erase discharge occurs, as in the odd field, and the wall charges formed by the reset discharge are neutralized.

The driving in the address period that follows is essentially the same as that in the odd field, except that the display and non-display slits are interchanged. That is, the scan pulse -Vy is applied in sequence to the odd-numbered scan electrodes, Y_1, Y_3, ..., Y_{2n-1}, while at the same time the data pulse Va corresponding to the input signal is selectively applied to the address electrodes A_j. At this time, in the even field, since the pulse Vx is applied only to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}, the write discharge is carried out only between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, and wall charges are thus accumulated on both electrodes. Next, the scan pulse -Vy is applied in sequence to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n}. Here again, since the data pulse Va is selectively applied to the address electrodes A_j, and the pulse Vx is now applied only to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}, the write discharge is carried out only between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., Y_{2n}-X_{2i-1}, and wall charges are thus accumulated on both electrodes.

In the sustain period that follows, the sustain discharge pulse Vs is applied alternately to the sustain electrodes X_i and scan electrodes Y_n hat form the display slits, as in the odd field, carrying out the sustain discharge in the discharge cells in which the write discharge has been carried out. More specifically, in the even field, the sustain discharge pulse is applied alternately between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, and also between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., X_{2n}-Y_{2i-1}, which form the display slits, but this pulse is in phase between the odd-numbered sustain electrodes and scan electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, and also between the even-numbered sustain electrodes and scan electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, which form the non-display slits.

As a modified example of the present embodiment, the electrodes to which the pulses Vs and -Vw are applied can be interchanged. That is, in the odd field, the negative polarity pulse -Vw is applied to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} and the positive polarity pulse Vs to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1}. At the same time, the positive polarity pulse Vs is applied to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i} and the negative polarity pulse -Vw to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n}. Likewise, in the even field, the negative polarity pulse -Vw is applied to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} and the positive polarity pulse Vs to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}. At the same time, the positive polarity pulse Vs is applied to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n} and the negative polarity pulse -Vw to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}.

Figures 2a and 2b are waveform diagrams illustrating a second embodiment of the present invention. This embodiment is the same as the first embodiment, except in respect of the reset period in each field.

In this embodiment, the slits where the voltage of Vs+Vw exceeding the inter-electrode discharge initiating voltage is applied, are provided alternately with the slits where the positive polarity pulse Vs and negative polarity pulse -Vw are applied

More specifically, in the odd field, between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, the scan electrodes Y_1, Y_3, ..., Y_{2n-1} are held at ground potential, and the pulse of Vs+Vw is applied to the sustain electrodes X_1, X_3, ..., X_{2i-1}, while between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, the negative polarity pulse -Vw is applied to the sustain electrodes X_2, X_4, ..., X_{2i} and the positive polarity pulse Vs to the scan electrodes Y_2, Y_4, ..., Y_{2n}. As a result, between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, and also between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., Y_{2n}-X_{2i-1}, the potential difference does not reach the discharge initiating voltage, so that discharge does not occur between them. At this time, it is desirable that a prescribed pulse Vaw be applied to the address electrodes A_j to prevent discharge from occurring between the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}, where Vs+Vw is applied, and the address electrodes A_j. As for the magnitude of the pulse Vaw, it should be set to a potential between an intermediate potential between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, X_{2i-1}-Y_{2n-1}, and an intermediate potential between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}. In the present embodiment, the pulse Vaw is set at the same potential as the data pulse Va to simplify driver circuitry.

The driving in the even field is essentially the same as that in the odd field, except that the display and non-display slits are interchanged; therefore, description thereof is omitted.

As a modified example of the second embodiment, the electrodes to which Vs+Vw is to be applied can be changed to the scan electrodes. That is, in the odd field, between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, the sustain electrodes X_1, X_3, ..., X_{2i-1} are held at ground potential, and the pulse of Vs+Vw is applied to the scan electrodes Y_1, Y_3, ..., Y_{2n-1}. In this case, between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, the positive polarity pulse Vs is applied to the sustain electrodes X_2, X_4, ..., X_{2i} and the

negative polarity pulse -Vw to the scan electrodes Y_2, Y_4, ..., Y_{2n}. This also applies to the even field.

Also, as a matter of course, it is possible to interchange the slits where Vs+Vw is applied and the slits where the positive polarity pulse Vs and negative polarity pulse -Vw are applied.

Figures 3a and 3b are waveform diagrams illustrating a third embodiment of the present invention. This embodiment is the same as the first and second embodiments, except in respect of the reset period.

In this embodiment, as in the second embodiment, the slits where the pulse exceeding the discharge initiating voltage is applied are provided alternately with the slits where the positive polarity pulse Vs and negative polarity pulse -Vw are applied. The difference in this embodiment is that a negative polarity pulse -Vyw (= - Vs - Vw) is applied as the pulse exceeding the discharge initiating voltage.

More specifically, in the odd field, between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, the negative polarity pulse -Vw is applied to the sustain electrodes X_1, X_3, ..., X_{2i-1} and the positive polarity pulse Vs to the scan electrodes Y_1, Y_3, ..., Y_{2n-1}, while between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, the sustain electrodes X_2, X_4, ..., X_{2i} is held at ground potential, and the negative polarity pulse -Vyw is applied to the scan electrodes Y_2, Y_4, ..., Y_{2n}. As a result, between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, and also between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., Y_{2n}-X_{2i-1}, the potential difference does not reach the discharge initiating voltage, so that discharge does not occur between them. In this case also, it is desirable that the prescribed pulse Vaw be applied to the address electrodes A_j to prevent a discharge from occurring between the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n}, where -Vyw is applied, and the address electrodes A_j. Here again, it is recommended that the pulse Vaw be set at a potential between an intermediate potential between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, X_{2i-1}-Y_{2n-1}, and an intermediate potential between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}. In this case, the pulse Vaw is set as a negative polarity pulse.

The driving in the even field is essentially the same as that in the odd field, except that the display and non-display slits are interchanged; therefore, a description thereof is omitted.

As a modified example of the third embodiment, the electrodes to which -Vyw is to be applied can be changed to the sustain electrodes. That is, in the odd field, between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, the scan electrodes Y_2, Y_4, ..., Y_{2n} are held at ground potential, and the pulse -Vyw is applied to the sustain electrodes X_2, X_4, ..., X_{2i}. In this case, between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, the positive polarity pulse Vs is applied to the sustain electrodes X_1, X_3, ..., X_{2i-1} and the negative polarity pulse -Vw to the scan electrodes Y_1, Y_3, ..., Y_{2n-1}. This also applies to the even field.

Also, it is possible to interchange the slits where the pulse -Vyw is applied and the slits where the positive polarity pulse Vs and negative polarity pulse -Vw are applied.

Figures 4a and 4b are waveform diagrams illustrating a fourth embodiment of the present invention. This embodiment is the same as the foregoing embodiments, except in respect of the reset period. A significant difference in this embodiment is that, while in the foregoing first to third embodiments the reset discharge is carried out simultaneously on all the display slits, in the present embodiment the reset discharge is carried out at different times. That is, in the present embodiment, the reset period is divided into a first reset period and a second reset period so that the reset discharge is carried out on the adjacent display slits in the different reset periods.

More specifically, in the first reset period, i.e., in the first half portion of the reset period of the odd field, the reset discharge is carried out between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, and in the second reset period corresponding to the second half portion, the reset discharge is carried out between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}. In the present embodiment, in the first reset period of the odd field, the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} is held at ground potential, and the pulse Vs+Vw exceeding the inter-electrode discharge initiating voltage is applied to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}. On the other hand, the even-numbered sustain electrodes X_2, X_4, ..., X_{2i} are held at ground potential, and the positive polarity pulse Vs is applied to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n}. As a result, the reset discharge takes place between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, but the discharge does not occur between the other electrodes since the potential difference between them does not reach the discharge initiating voltage. In the second reset period that follows, the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n} are held at ground potential, and the pulse Vs+Vw exceeding the inter-electrode discharge initiating voltage is applied to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}, thereby causing the reset discharge to occur between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}. On the other hand, the applied voltage to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} is reduced from Vs+Vw to Vs while holding the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} at ground potential.

Here again, similarly to the first period, it would seem appropriate to apply the pulse Vs to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} to prevent a discharge from occurring between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, but if this were done, a sustain discharge would occur between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, because of the wall charges formed by the reset discharge in the first reset period. For this reason, the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} are held at ground, potential. However, since positive wall charges are accumulated on the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} by the reset discharge in the first reset period, and the potential difference between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i} is lowered, discharge does not occur between them. Further, the reason the pulse Vs is applied to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} is that if they were lowered to ground potential, a self-erase discharge would occur between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, neutralizing the wall charges that should lower the potential difference between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}. In the present embodiment, the self-erase discharge occurs simultaneously in all the display slits after the end of the second reset period.

For the same reason as described in the foregoing embodiments, it is desirable that the prescribed pulse Vaw be applied to the address electrodes A_j throughout the first and second reset periods. Here again, it is recommended that the pulse Vaw be set at a potential between an intermediate potential between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, X_{2i-1}-Y_{2n-1}, and an intermediate potential between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}. In the present embodiment, the pulse Vaw is set to the same potential as the data pulse Va.

The driving in the even field is essentially the same as that in the odd field, except that the display and non-display slits are interchanged; therefore, description thereof is omitted.

As a modified example of the fourth embodiment, the electrodes to which the pulse Vs+Vw is to be applied in the first reset period can be changed to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1}. In this case, the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} are held at ground potential, and the pulse Vs is applied to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}. In the second reset period that follows, the pulse Vs+Vw is applied to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1}, while the potential of the pulse Vs+Vw being applied to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} is reduced to Vs. The even-numbered sustain electrodes X_2, X_4, ..., X_{2i} and the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} are both at ground potential. The driving in the even field is essentially the same as that in the odd field, except that the display and non-display slits are interchanged.

Further, in the first reset period of the odd field, the pulse Vs+Vw may be applied between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, and the pulse Vs applied between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}; in this way, the display slits where the discharge is caused can be interchanged between the first and second reset periods.

Figures 5a and 5b are waveform diagrams illustrating a fifth embodiment of the present invention. In this embodiment also, the reset discharge is carried out on adjacent display slits at different times by dividing the reset period. This embodiment may be viewed as a development of the foregoing fourth embodiment.

More specifically, in the first reset period of the odd field, the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} is held at ground potential, and the positive polarity pulse Vs+Vw exceeding the inter-electrode discharge initiating voltage is applied to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}, as in the fourth embodiment. On the other hand, the positive polarity pulse Vs is applied to both the even-numbered sustain electrodes X_2, X_4, ..., X_{2i} and the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n}. As a result, the reset discharge takes place only between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, while preventing the discharge from occurring between the other electrodes. In this case, the positive pulse Vs+Vw may be applied to the odd-numbered scan electrodes X_1, Y_3, ..., Y_{2n-1}. In the second reset period that follows, the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n} are held at ground potential, and the positive polarity pulse Vs+Vw is applied to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}. On the other hand, the positive polarity pulse Vs is applied to both the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} and the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1}. As a result, the reset discharge takes place only between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, while preventing the discharge from occurring between the other electrodes. In this case, the positive polarity pulse Vs+Vw may be applied to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n}.

In the present embodiment, since the first and second reset periods are completely independent processes, the pulses applied in the respective periods are separated in time. As a result, in the present embodiment, the self-erase discharge occurs separately at the end of each period. Further, the pulse Vaw is applied to the address electrodes A_j, as in the foregoing embodiments, but this pulse is also separated between the first and second reset periods.

The driving in the even field is essentially the same as that in the odd field, except that the display and non-display slits are interchanged.

Figures 6a and 6b are waveform diagrams illustrating a sixth embodiment of the present invention. In this embodiment also, the reset discharge is carried out on adjacent display slits at different times by dividing the reset period. The feature of this embodiment is that the same pulses are applied to the adjacent display slits at different times.

More specifically, in the first reset period of the odd field, the positive polarity pulse Vs is applied to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} and the negative polarity pulse -Vw to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1}. At this time, the even-numbered sustain electrodes X_2, X_4, ..., X_{2i} and scan electrodes Y_2, Y_4, ..., Y_{2n}, which form the adjacent display slits, are both held at ground potential. As a result, the reset discharge takes place only between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, while preventing the discharge from occurring between the other electrodes. In the second reset period that follows, the positive polarity pulse Vs is applied to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i} and the negative polarity pulse -Vw to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n}. At this time, the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} and scan electrodes Y_1, Y_3, ..., Y_{2n-1}, which form the adjacent display slits, are both held at ground potential. As a result, the reset discharge takes place only between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}, while preventing the discharge from occurring between the other electrodes.

On the other hand, in the first reset period of the even field, the negative polarity pulse -Vw is applied to the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n} and the positive polarity pulse Vs is applied to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}. At this time, the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} and the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}, which form the adjacent display slits, are both held at ground potential. As a result, the reset discharge takes place only between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., Y_{2n}-X_{2i-1}, while preventing the discharge from occurring between the other electrodes. In the second reset period that follows, the negative polarity pulse -Vw is applied to the odd-numbered scan electrodes Y_1, Y_3, ..., Y_{2n-1} and the positive polarity pulse Vs to the even-numbered sustain electrodes X_2, X_4, ..., X_{2i}. At this time, the even-numbered scan electrodes Y_2, Y_4, ..., Y_{2n} and the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1}, which form the adjacent display slits, are both held at ground potential. As a result, the reset discharge takes place only between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i}, while preventing the discharge from occurring between the other electrodes. In the present embodiment, since the pulse applied to each electrode has a voltage value less than the discharge initiating voltage, there is no need to apply a pulse to the address electrodes A_j.

It should be noted here that the same pulse is applied to the same electrode in the respective reset periods of the odd and even fields. That is, in the reset period, whether in the odd field or in the even field, the pulse applied to the sustain electrodes X_i is Vs, and the pulse applied to the scan electrodes Y_n is - Vw. Accordingly, in the present embodiment, it is possible to select the slits where the reset discharge is to be carried out, depending on whether the reset pulse to be applied to each electrode is applied in the first reset period or in the second reset period. Here, the pulses applied to the sustain electrodes X_i and scan electrodes Y_n, respectively, can be interchanged. For example, in the first reset period of the odd field, the negative polarity pulse -Vw is applied to the odd-numbered sustain electrodes X_1, X_3, ..., X_{2i-1} and the positive polarity pulse Vs applied to the scan electrodes Y_1, Y_3, ..., Y_{2n-1}.

Figures 7a and 7b are waveform diagrams illustrating a seventh embodiment of the present invention. This embodiment can be viewed as a development of the sixth embodiment in that the slits between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i} are chosen as the display slits where the reset discharge is carried out in the first reset period of the even field.

In this embodiment, however, the timing at which the second reset period is carried out is changed and the second reset period is initiated at a point halfway through the address period. More specifically, first the reset discharge in the first reset period is carried out between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}, and then an address discharge is carried out in sequence between the same electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1}. After that, the reset discharge in the second reset period is carried out between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n-1}, and then an address discharge is carried out in sequence between the same electrodes X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}. In this way, in the present embodiment, not only the reset period but the address period is also carried out at different times on the adjacent display splits. In the even field also, the address period is split in the same way as in the odd field.

The method of splitting the address period according to the present embodiment can be applied to any of the foregoing embodiments except the fourth embodiment. The first to third embodiments have been described based on the premise that the reset discharge is carried out at the same time on all the display slits, but it is possible to provide the reset period for one or the other of the adjacent display slits at some point halfway through the address period without changing

the pulse applied to each electrode. In the fourth embodiment, on the other hand, since the wall charges formed in the first reset period are used in the second reset period, the two reset periods must be carried out in succession,

When a transition is made from the odd field to the even field or from the even field to the odd field, there occur cases where the wall charges remaining after the end of the discharge in the immediately preceding subfield cannot be erased completely. For example, consider the case where a transition is made from the odd field to the even field. In the odd field, the reset discharge is carried out between the odd-numbered scan electrodes and sustain electrodes, X_1-Y_1, X_3-Y_3, ..., X_{2i-1}-Y_{2n-1} and also between the even-numbered scan electrodes and sustain electrodes, X_2-Y_2, X_4-Y_4, ..., X_{2i}-Y_{2n}. Accordingly, the residual wall charges tend to remain in inner regions between the respective electrodes. Reset discharge is then carried out in the reset period of the first subfield in the even field. This reset discharge is carried out between the odd-numbered scan electrodes and even-numbered sustain electrodes, Y_1-X_2, Y_3-X_4, ..., Y_{2n-1}-X_{2i} and also between the even-numbered scan electrodes and odd-numbered sustain electrodes, Y_2-X_3, Y_4-X_5, ..., Y_{2n}-X_{2i-1}. In this case, the reset discharge is carried out in inner regions between the respective electrodes, thus tending to make it difficult to erase the wall charges remaining in the outer regions, that is, the inner regions between the electrodes where the discharge was carried out in the immediately preceding subfield.

Accordingly, in the embodiments of the present invention, it is desirable that when a transition is made from the odd field to the even field or from the even field to the odd field, the reset discharge be carried out between all the electrodes, including the non-display slits in the new field, as in the previously considered driving method described with reference to Figure 13, but only in the first subfield of the new field. For example, in the first subfield of the odd field or even field, the pulse Vs+Vw exceeding the inter-electrode discharge initiating voltage should be applied to all the sustain electrodes X_i while holding all the scan electrodes Y_n at ground potential.

Figure 8 is a circuit diagram showing an X-side driver embodying the present invention, wherein reference numeral 3 is an X-common driver, 33 is an X positive write circuit, 34 is an X negative write circuit A, and 35 is an X negative write circuit B. Actually, an X-common driver A connected to the odd-numbered electrodes X_o and an X-common driver B connected to the even-numbered electrodes X_e are provided as the X-common driver. Of the X positive write circuit, X negative write circuit A, and X negative write circuit B, in the first embodiment the X negative write circuit A is used when connecting to the even-numbered electrodes X_e; in the second embodiment, the X positive write circuit is used when connecting to the odd-numbered electrodes X_o and the X negative write circuit A when connecting to the even-numbered electrodes X_e; in the third embodiment, the X negative write circuit A and X negative write circuit B are used when connecting to the odd-numbered electrodes X_o; and in the fourth and fifth embodiment, the X positive write circuit is used for the drivers connected to all the drivers. None of the X positive write circuit, X negative write circuit A, and X negative write circuit B are needed in the first embodiment when connecting to the odd-numbered electrodes X_o, in the third embodiment when connecting to the even-numbered electrodes X_e, and in the sixth and seventh embodiments regardless of the connection.

In the X-common driver, a switch element SW1 and a switch element SW2 are connected in series between a power supply line of potential Vs and a ground line, and diodes D2 and D3 are connected in parallel with the switch elements SW1 and SW2, respectively. Between the switch element SW1 and potential Vs, there is connected a diode D1 with its anode on the potential Vs side. One terminal of a switch element SW3 is connected to the anode of a diode D19, while one terminal of a switch element SW4 is connected to the cathode of a diode D20. The cathode of the diode D19 and the anode of the diode D20 are connected in common, and a power supply line of potential Vx is connected to the other terminals of the switch elements SW3 and SW4. Diodes D4 and D5 are connected in parallel with the switch elements SW3 and SW4, respectively. The cathode of the diode D19 and the anode of the diode D20, which are connected in common, are connected to the node between the switch elements SW1 and SW2 to provide an output of the X-common driver 3.

In the X positive write circuit, a switch element SW5 and a switch element SW6 are connected in series between a power supply line of potential Vw and the ground line, and diodes D6 and D7 are connected in parallel with the switch elements SW5 and SW6, respectively. To the node between the switch elements SW5 and SW6 is connected one end of a capacitor C1 whose other end is connected to the node between the switch element SW1 and diode D1 in the X-common driver 3.

In the X negative write circuit A, one terminal of a switch element SW7 is connected to the output of the X-common driver, while the other terminal thereof is connected to the anode of a diode D21. Further, one terminal of a switch element SW8 is connected to a power supply line of -Vw, while the other terminal thereof is connected to the cathode of the diode D21. Diodes D8 and D9 are connected in parallel with the switch elements SW7 and SW8, respectively.

The X negative write circuit B comprises a switch element SW9, connected between a power supply line of - Vyw and the node between the switch element SW7 and diode D21 in the X negative write circuit A, and a diode D10 connected in parallel with the switch element SW9.

The node between the X negative write circuit A and the X negative write circuit B serves an output terminal of the X-side driver for connection to the even-numbered sustain electrodes X_o or odd-numbered sustain electrodes X_e. However, when the X negative write circuit A is not used, the output of the X-common driver 3 serves as the output terminal of the X-side driver.

In the reset period, SW1, SW8, and SW9 are turned on as needed, to produce the potentials Vs, -Vw, and -Vyw. When producing Vs+Vw, SW5 is turned on so that the potential Vw is superimposed on the potential Vs being applied to one end of the capacitor C1.

The X negative write circuit A isolates the X-common driver 3 from the potential -Vw by using the switch element SW7. This is done to prevent feed-through current from flowing from the ground potential to the power supply line of -Vw through the diode D3 and through the switch element SW8 when the switch element SW8 is turned on. When the X negative write circuit A is put in operation, the feed-through current can be prevented by turning off the switch element SW7.

In the address period, the pulse Vx for selecting the display slits is generated via the switch elements SW3 and SW4. Here, the two switch elements SW3 and SW4 are used to supply the potential Vx because it has been found that if only one switch element is used, the potential of the sustain electrodes X_i varies through inter-electrode capacitance as the address pulse Va is applied to the address electrodes A_j. By taking the output from the node between the two switch elements SW3 and SW4 connected to the power supply line Vx, the variation in the potential of the sustain electrodes X_i can be prevented.

In the sustain period, the switch element SW1 is turned on as needed, to produce the sustain discharge pulse Vs.

In this embodiment, each switch element is constructed from a D-FET which is a power FET capable of supplying large power. The D-FET (shown by a schematic representation for the X-side driver only) passes current only in one direction since essentially its source and drain are fixed, but at the same time, has a parasitic diode directed in the opposite direction. Accordingly, by using the D-FET, the diode connected in parallel with each element can be omitted.

Figure 9 is a circuit diagram showing Y-side drivers embodying the present invention, wherein reference numeral 4 is a Y-scan driver, 5 is a Y-common driver, 53 is a Y positive write circuit, 54 is a Y negative write circuit A, and 55 is a Y negative write circuit B. Actually, a Y-common driver A connected to the odd-numbered electrodes Y_o and a Y-common driver B connected to the even-numbered electrodes Y_e are provided as the Y-common driver. The Y-scan drivers are connected to individual scan electrodes Y_i, one driver driving each electrode independently. The Y-common driver is connected in common to the Y-scan drivers connected to the odd-numbered scan electrodes Y_o or the Y-scan drivers connected to the even-numbered scan electrodes Y_e, and drives the odd-numbered scan electrodes Y_o or the even-numbered scan electrodes Y_e. Of the Y positive write circuit, Y negative write circuit A, and Y negative write circuit B, in the first, sixth, and seventh embodiments the Y negative write circuit A is used for the drivers connected to all the electrodes; in the second embodiment, the Y positive write circuit is used when connecting to the odd-numbered scan electrodes Y_o and the Y negative write circuit A when connecting to the even-numbered electrodes Y_e; in the third embodiment, the Y negative write circuit A is used when connecting to the odd-numbered scan electrodes Y_o and the Y negative write circuit B when connecting to the even-numbered electrodes Y_e; and in the fourth embodiment, the Y positive write circuit is used for the drivers connected to all the electrodes. In the fifth embodiment, none of the Y positive write circuit, Y negative write circuit A, and Y negative write circuit B are needed.

In the Y-common driver, one terminal of a switch element SW10 is connected to the ground line, while the other terminal thereof is connected to the power supply line of potential Vs through the anode and cathode of a diode D11 and also to line FVH through the anode and cathode of a diode D12. The line FVH passes through the anode and cathode of a diode D13 and is connected to a power supply line of potential -Vsc through a switch element SW11. The anode of a diode D14 is connected to the power supply line of potential Vs, while the cathode thereof is connected to one terminal of a switch element SW12. The other terminal of the switch element SW12 is connected to the ground line through the anode and cathode of a diode D15 and also to line FLG via a switch element SW13. The line FLG is connected to a power supply line of -Vy via a switch element SW14.

In the Y-scan driver, the anode of a diode D16, the cathode of a diode D17, one terminal of a switch element SW15, and one terminal of a switch element SW16 are connected in common to the associated scan electrode Y_i, and the cathode of the diode D16 and the other terminal of the switch SW15 are connected to the line FVH, while the anode of the diode D17 and the other terminal of the switch SW16 are connected to the line FLG.

In the Y positive write circuit, a switch element SW17 and a switch element SW18 are connected in series between the power supply line of potential Vw and the ground line, and one end of a capacitor C2 is connected to the node between the switch elements SW17 and SW18. The other end of the capacitor C2 is connected to the cathode of the diode D14 in the Y-common driver.

The Y negative write circuit A includes a diode D18 whose cathode is connected to the power supply line of potential -Vw via a switch element SW19 and whose anode is connected to the line FVH of the Y-common driver.

The Y negative write circuit B includes a switch element SW20 whose one end is connected to the power supply line of potential -Vyw and whose other end is connected to the line FVH of the Y-common driver.

In the reset period, the switch element SW19 or SW20 is turned on as needed, causing current to flow via the diode D16 to the power supply line of -Vw or -Vyw to drive the odd-numbered electrodes Y_o or the even-numbered electrodes Y_e to the potential -Vw or -Vyw. When supplying the potential Vs, the switch elements SW12 and SW13 are turned on to supply the potential Vs via the diodes D14 and D17. When supplying the potential Vs+Vw, the switch element SW17 is turned on so that the potential Vw is superimposed on the potential Vs being applied to the capacitor C2, and the resulting Vs+Vw is supplied via the diode D17 to the odd-numbered electrodes Y_o or the even-numbered electrodes Y_e.

In the address period, by turning the switch elements SW11 and SW14 on and the other switch elements off, the deselect potential -Vsc and select potential -Vy are applied to the scan electrode Y_i. At this time, the switch SW13 is turned off to prevent current from flowing to the power supply line of potential -Vy through the diode D15. In this condition, by turning on the switch element SW16 the potential -Vy for the scan pulse is applied to the, scan electrode Y_i, and by turning on the switch element SW15 the deselect potential -Vsc is applied to the scan electrode Y_i. This operation is performed in sequence for the odd-numbered scan electrodes Y_o and even-numbered scan electrodes Y_e.

When lowering a positive potential scan electrode Y_i to 0 V, the switch element SW10 is turn on and the other switch elements are turned off. This causes the current for bringing the scan electrode Y_i to 0 V to flow from the scan electrode Y_i and to pass through the diodes D16 and D12 and via the switch element SW10. When raising a negative potential scan electrode Y_i to 0 V, the switch element SW13 is turned on and the other switch elements are turned off. This causes the current for driving the scan electrode Y_i to 0 V to flow from the diode D15 and to pass through the switch element SW13 and diode D17.

In the sustain period, by turning the switch elements SW12 and SW13 on and the other switch elements off, the potential Vs is applied to the scan electrode Y_i through the diode D14, switch elements SW12 and SW13, and diode D17.

Claims

1. A method of driving a plasma display panel in which a plurality of sustain electrodes X_i and a plurality of scan electrodes Y_n are arranged parallel to each other on a first substrate to form display lines, and a plurality of address electrodes A_j electrically isolated from said sustain electrodes X_i and said scan electrodes Y_n are arranged on a second substrate, spaced apart from said first substrate, so as to cross said sustain electrodes X_i and said scan electrodes Y_n at a distance to form discharge cells at the crossing regions, the method comprising:

   an odd field in which a display is produced between odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, and an even field in which a display is produced between the odd-numbered sustain electrodes X_{2i-1} and even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, each of said odd and even fields including:
   a reset period in which a reset discharge is carried out in a plurality of said discharge cells by applying voltages to said sustain electrodes X_i, said scan electrodes Y_n, and said address electrodes A_j to accomplish a uniform charge distribution among said plurality of discharge cells;
   an address period in which a write discharge is carried out in selected discharge cells between said scan electrodes Y_n and said address electrodes A_j, thereby performing to write display data selectively; and
   a sustain discharge period in which sustain discharge pulses are applied between said sustain electrodes X_i and said scan electrodes Y_n, thereby causing a discharge glow for said display at said discharge cells in which the writing has been performed in said address period, wherein
   potential differences between said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} and between said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1} during the reset period of said odd field, and potential differences between said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} during the reset period of said even field, are each held below a discharge initiating voltage between the respective electrodes.

2. The method according to claim 1, wherein said reset discharge in said odd field is carried out between said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} at the same time, and

   said reset discharge in said even field is carried out between said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan

electrodes Y_{2n} and between said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1} at the same time.

3. The method according to claim 2, wherein in said odd and even fields, said reset discharge is accomplished by applying pulses of positive or negative polarity to said sustain electrodes X_i and said scan electrodes Y_n, the pulses applied to said sustain electrodes X_i and said scan electrodes Y_n being such that:

in said odd field, said pulses are opposite in polarity between said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, and are identical in polarity between said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} and between said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1}; and in said even field, said pulses are opposite in polarity between said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} and between said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1}, and are identical in polarity between said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}.

4. The method according to claim 3, wherein said reset discharge in said odd field is accomplished by applying a first pulse of positive polarity to said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} and a second pulse of negative polarity to said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1}, and

said reset discharge in said even field is accomplished by applying said first pulse of positive polarity to said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and said second pulse of negative polarity to said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}.

5. The method according to claim 3, wherein said reset discharge in said odd field is accomplished by applying a first pulse of positive polarity to said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1} and a second pulse of negative polarity to said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n}, and

said reset discharge in said even field is accomplished by applying said first pulse of positive polarity to said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} and said second pulse of negative polarity to said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1}.

6. The method according to claim 4, wherein during said reset discharge in said odd and even fields, said address electrodes A_j are held at ground potential.

7. The method according to claim 2, wherein said reset discharge in said odd field is accomplished by applying first and second pulses of opposite polarities respectively to said sustain electrodes X_i and said scan electrodes Y_n belonging to either one electrode group consisting of said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} or consisting of said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, while applying a third pulse of positive polarity greater than said discharge initiating voltage to either said sustain electrodes X_i or said scan electrodes Y_n belonging to the other electrode group, and

said reset discharge in said even field is accomplished by applying said first and second pulses of opposite polarities respectively to said sustain electrodes X_i and said scan electrodes Y_n belonging to either one electrode group consisting of said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} or consisting of said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1}, while applying said third pulse of positive polarity greater than said discharge initiating voltage to either said sustain electrodes X_i or said scan electrodes Y_n belonging to the other electrode group.

8. The method according to claim 7, wherein in said one electrode group in said odd field, said first pulse with a positive polarity is applied to said scan electrodes Y_n and said second pulse with a negative polarity to said sustain electrodes X_i, while in said other electrode group, said third pulse of positive polarity is applied to said sustain electrodes X_i, and

in said one electrode group in said even field, said first pulse of positive polarity is applied to said sustain electrodes X_i and said second pulse of negative polarity to said scan electrodes Y_n, while in said other electrode group, said third pulse of positive polarity is applied to said scan electrodes Y_n.

9. The method according to claim 8, wherein in said other electrode group in said odd field, said scan electrodes Y_n are held at ground potential, and in said other electrode group in said even field, said sustain electrodes X_i are held at ground potential.

10. The method according to claim 7, wherein in said one electrode group in said odd field, said first pulse with a positive polarity is applied to said sustain electrodes X_i and said second pulse with a negative polarity to said scan electrodes Y_n, while in said other electrode group, said third pulse of positive polarity is applied to said scan electrodes Y_n, and

in said one electrode group in said even field, said first pulse of positive polarity is applied to said scan electrodes Y_n and said second pulse of negative polarity to said sustain electrodes X_i, while in said other electrode group, said third pulse of positive polarity is applied to said sustain electrodes X_i.

11. The method according to claim 10, wherein in said other electrode group in said odd field, said sustain electrodes X_i are held at ground potential, and in said other electrode group in said even field, said scan electrodes Y_n are held at ground potential.

12. The method according to claim 8, wherein during said reset discharge in said odd and even fields, said address electrodes A_j are held at a potential not lower than an intermediate potential between the electrodes of said one electrode group but not higher than an intermediate potential between the electrodes of said other group.

13. The method according to claim 2, wherein said reset discharge in said odd field is accomplished by applying first and second pulses of opposite polarities respectively to said sustain electrodes X_i and said scan electrodes Y_n belonging to either one electrode group consisting of said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} or consisting of said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, while applying a fourth pulse of negative polarity greater than said discharge initiating voltage to either said sustain electrodes X_i or said scan electrodes Y_n belonging to the other electrode group, and

said reset discharge in said even field is accomplished by applying said first and second pulses of opposite polarities respectively to said sustain electrodes X_i and said scan electrodes Y_n belonging to either one electrode group consisting of said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} or consisting of said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1}, while applying said fourth pulse of negative polarity greater than said discharge initiating voltage to either said sustain electrodes X_i or said scan electrodes Y_n belonging to the other electrode group.

14. The method according to claim 13, wherein in said one electrode group in said odd field, said first pulse with a positive polarity is applied to said scan electrodes Y_n and said second pulse with a negative polarity to said sustain electrodes X_i, while in said other electrode group, said fourth pulse of negative polarity is applied to said scan electrodes Y_n, and

in said one electrode group in said even field, said first pulse of positive polarity is applied to said sustain electrodes X_i and said second pulse of negative polarity to said scan electrodes Y_n, while in said other electrode group, said fourth pulse of negative polarity is applied to said sustain electrodes X_i.

15. The method according to claim 14, wherein in said other electrode group in said odd field, said sustain electrodes X_i are held at ground potential, and in said other electrode group in said even field, said scan electrodes Y_n are held at ground potential.

16. The method according to claim 13, wherein in said one electrode group in said odd field, said first pulse with a positive polarity is applied to said sustain electrodes X_i and said second pulse with a negative polarity to said scan electrodes Y_n, while in said other electrode group, said fourth pulse of negative polarity is applied to said sustain electrodes X_i, and

in said one electrode group in said even field, said first pulse of positive polarity is applied to said scan electrodes Y_n and said second pulse of negative polarity to said sustain electrodes X_i, while in said other electrode group, said fourth pulse of negative polarity is applied to said scan electrodes Y_n.

17. The method according to claim 16, wherein in said other electrode group in said odd field, said scan electrodes Y_n are held at ground potential, and in said other electrode group in said even field, said sustain electrodes X_i are held at ground potential.

18. The method according to claim 15, wherein during said reset discharge in said odd and even fields, said address electrodes A_j are held at a potential not lower than a potential intermediate between the electrodes of said other electrode group but not higher than a potential intermediate between the electrodes of said one group.

19. The method according to claim 1, wherein said reset discharge in said odd field is carried out between said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} at different times, and

said reset discharge in said even field is car-

ried out between said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} and between said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1} at different times.

20. The method according to claim 19, wherein in said odd and even fields, said reset period including a first reset period and a second reset period, and wherein:

in said odd field, a reset discharge is carried out in said first reset period between the electrodes belonging to either one electrode group consisting of said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} or consisting of said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, after which a reset discharge is carried out between the electrodes of the other electrode group in said second reset period that follows,

then said write discharge is carried out in sequence to produce a display between the electrodes of said one electrode group, after which said write discharge is carried out in sequence to produce a display between the electrodes of said other electrode group, and

finally said sustain discharge is carried out between the electrodes of said one electrode group and between the electrodes of said other electrode group; and

in said even field, a reset discharge is carried out in said first reset period between the electrodes belonging to either one electrode group consisting of said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} or consisting of said even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, after which a reset discharge is carried out between the electrodes of the other electrode group in said second reset period that follows,

then said write discharge is carried out in sequence to produce a display between the electrodes of said one electrode group, after which said write discharge is carried out in sequence to produce a display between the electrodes of said other electrode group, and

finally said sustain discharge is carried out between the electrodes of said one electrode group and between the electrodes of said other electrode group.

21. The method according to claim 20, wherein in said odd field, in said first reset period a third pulse of positive polarity greater than said discharge initiating voltage is applied between the electrodes of said one electrode group, and then in said second reset period, said third pulse of positive polarity greater than said discharge initiating voltage is applied between the electrodes of said other electrode group, and

in said even field, in said first reset period said third pulse of positive polarity greater than said discharge initiating voltage is applied between the electrodes of said one electrode group, and then in said second reset period, said third pulse of positive polarity greater than said discharge initiating voltage is applied between the electrodes of said other electrode group.

22. The method according to claim 21, wherein in said odd field, in said first reset period said third pulse is applied to the sustain electrodes X_i of said one electrode group, while at the same time applying a first pulse of positive polarity to the scan electrodes Y_n of said other electrode group, and then in said second reset period, said third pulse is applied to the sustain electrodes X_i of said other electrode group, while at the same time applying said first pulse to the sustain electrodes X_i of said one electrode group, and

in said even field, in said first reset period said third pulse is applied to the scan electrodes Y_n of said one electrode group, while at the same time applying said first pulse of positive polarity to the sustain electrodes X_i of said other electrode group, and then in said second reset period, said third pulse is applied to the scan electrodes Y_n of said other electrode group, while at the same time applying said first pulse to the scan electrodes Y_n of said one electrode group.

23. The method according to claim 21, wherein in said odd field, in said first reset period said third pulse is applied to the scan electrodes Y_n of said one electrode group, while at the same time applying a first pulse of positive polarity to the sustain electrodes X_i of said other electrode group, and then in said second reset period, said third pulse is applied to the scan electrodes Y_n of said other electrode group, while at the same time applying said first pulse to the scan electrodes Y_n of said one electrode group, and

in said even field, in said first reset period said third pulse is applied to the sustain electrodes X_i of said one electrode group, while at the same time applying said first pulse of positive polarity to the scan electrodes Y_n of said other electrode group, and then in said second reset period, said third pulse is applied to the sustain electrodes X_i of said other electrode group, while at the same time applying said first pulse to the sustain electrodes X_i of said one electrode group.

24. The method according to claim 22, wherein during

said reset periods in said odd and even fields, said address electrodes A_j are held at a potential between an intermediate potential between the electrodes of said one electrode group and an intermediate potential between the electrodes of said other electrode group.

25. The method according to claim 19, wherein in said odd and even fields, said reset period including a first reset period and a second reset period, and wherein:

in said odd field, a reset discharge is carried out in said first reset period between the electrodes belonging to either one electrode group consisting of said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} or consisting of said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, after which said write discharge is carried out in sequence to produce a display between the electrodes of said one electrode group,
then, a reset discharge is carried out between the electrodes of the other electrode group in said second reset period, after which said write discharge is carried out in sequence to produce a display between the electrodes of said other electrode group, and
finally said sustain discharge is carried out between the electrodes of said one electrode group and between the electrodes of said other electrode group; and
in said even field, a reset discharge is carried out in said first reset period between the electrodes belonging to either one electrode group consisting of said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} or consisting of said even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, after which said write discharge is carried out in sequence to produce a display between the electrodes of said-one electrode group,
then, a reset discharge is carried out between the electrodes of the other electrode group in said second reset period, after which said write discharge is carried out in sequence to produce a display between the electrodes of said other electrode group, and
finally said sustain discharge is carried out between the electrodes of said one electrode group and between the electrodes of said other electrode group.

26. The method according to claim 20, wherein in said odd field, in said first reset period a third pulse of positive polarity greater than said discharge initiating voltage is applied between the electrodes of said one electrode group, while at the same time applying a first pulse of positive polarity to said sustain electrodes X_i and scan electrodes Y_n of said other electrode group, and then in said second reset period, said third pulse of positive polarity greater than said discharge initiating voltage is applied between the electrodes of said other electrode group, while at the same time applying said first pulse of positive polarity to said sustain electrodes X_i and scan electrodes Y_n of said one electrode group, and

in said even field, in said first reset period said third pulse of positive polarity greater than said discharge initiating voltage is applied between the electrodes of said one electrode group, while at the same time applying said first pulse of positive polarity to said sustain electrodes X_i and scan electrodes Y_n of said other electrode group, and then in said second reset period, said third pulse of positive polarity greater than said discharge initiating voltage is applied between the electrodes, of said other electrode group, while at the same time applying said first pulse of positive polarity to said sustain electrodes X_i and scan electrodes Y_n of said one electrode group.

27. The method according to claim 20, wherein in said odd field, in said first reset period first and second pulses of opposite polarities are respectively applied to said sustain electrodes X_i and scan electrodes Y_n of said one electrode group, and in said second reset period, said first and second pulses of opposite polarities are respectively applied to said sustain electrodes X_i and scan electrodes Y_n of said other electrode group, and

in said even field, in said first reset period said first and second pulses of opposite polarities are respectively applied to said sustain electrodes X_i and scan electrodes Y_n of said one electrode group, and in said second reset period, said first and second pulses of opposite polarities are respectively applied to said sustain electrodes X_i and scan electrodes Y_n of said other electrode group.

28. The method according to claim 1, wherein said odd and even fields each having a plurality of subfields each having said reset period, said address period, and said sustain discharge period, and

when a transition is made from said odd field to said even field or from said even field to said odd field, in the first of said plurality of subfields potential differences between all the sustain electrodes X_i and scan electrodes Y_n are held not lower than the discharge initiating voltage between the respective electrodes.

29. A plasma display panel in which a plurality of sus-

tain electrodes X_i and a plurality of scan electrodes Y_n are arranged parallel to each other on a first substrate in corresponding to display lines, and a plurality of address electrodes A_j electrically isolated from said sustain electrodes X_i and said scan electrodes Y_n are arranged on a second substrate, spaced apart from said first substrate, so as to cross said sustain electrodes X_i and said scan electrodes Y_n at a distance to form discharge cells at the crossing regions, the panel comprising:

means for providing an odd field in which a display is produced between odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, and an even field in which a display is produced between the odd-numbered sustain electrodes X_{2i-1} and even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, each of said odd and even fields including:
a reset period in which a reset discharge is carried out in a plurality of said discharge cells by applying voltages to said sustain electrodes X_i, said scan electrodes Y_n, and said address electrodes A_j to accomplish a uniform charge distribution among said plurality of discharge cells;
an address period in which a write discharge is carried out in selected discharge cells between said scan electrodes Y_n and said address electrodes A_j, thereby performing to write display data selectively; and
a sustain discharge period in which sustain discharge pulses are applied between said sustain electrodes X_i and said scan electrodes Y_n, thereby causing a discharge glow for said display at said discharge cells in which the writing has been performed in said address period, wherein
potential differences between said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} and between said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1} during the reset period of said odd field, and potential differences between said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} during the reset period of said even field, are each held below a discharge initiating voltage between the respective electrodes.

30. A display apparatus comprising:

a plasma display panel in which a plurality of sustain electrodes X_i and a plurality of scan electrodes Y_n are arranged parallel to each other on a first substrate in corresponding to display lines, and a plurality of address electrodes A_j electrically isolated from said sustain electrodes X_i and said scan electrodes Y_n are arranged on a second substrate, spaced apart from said first substrate, so as to cross said sustain electrodes X_i and said scan electrodes Y_n at a distance to form discharge cells at the crossing regions; and
drive circuits for respectively driving said sustain electrodes X_i, said scan electrodes Y_n, and said address electrodes A_j, wherein
there are provided an odd field in which a display is produced between odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n}, and an even field in which a display is produced between the odd-numbered sustain electrodes X_{2i-1} and even-numbered scan electrodes Y_{2n} and between the even-numbered sustain electrodes X_{2i} and odd-numbered scan electrodes Y_{2n-1}, each of said odd and even fields including:
a reset period in which a reset discharge is carried out in a plurality of said discharge cells by applying voltages to said sustain electrodes X_i, said scan electrodes Y_n, and said address electrodes A_j to accomplish a uniform charge distribution among said plurality of discharge cells;
an address period in which a write discharge is carried out in selected discharge cells between said scan electrodes Y_n and said address electrodes A_j, thereby performing to write display data selectively; and
a sustain discharge period in which sustain discharge pulses are applied between said sustain electrodes X_i and said scan electrodes Y_n, thereby causing a discharge glow for said display at said discharge cells in which the writing has been performed in said address period, wherein
potential differences between said odd-numbered sustain electrodes X_{2i-1} and said even-numbered scan electrodes Y_{2n} and between said even-numbered sustain electrodes X_{2i} and said odd-numbered scan electrodes Y_{2n-1} during the reset period of said odd field, and potential differences between said odd-numbered sustain electrodes X_{2i-1} and scan electrodes Y_{2n-1} and between said even-numbered sustain electrodes X_{2i} and scan electrodes Y_{2n} during the reset period of said even field, are each held below a discharge initiating voltage

between the respective electrodes.

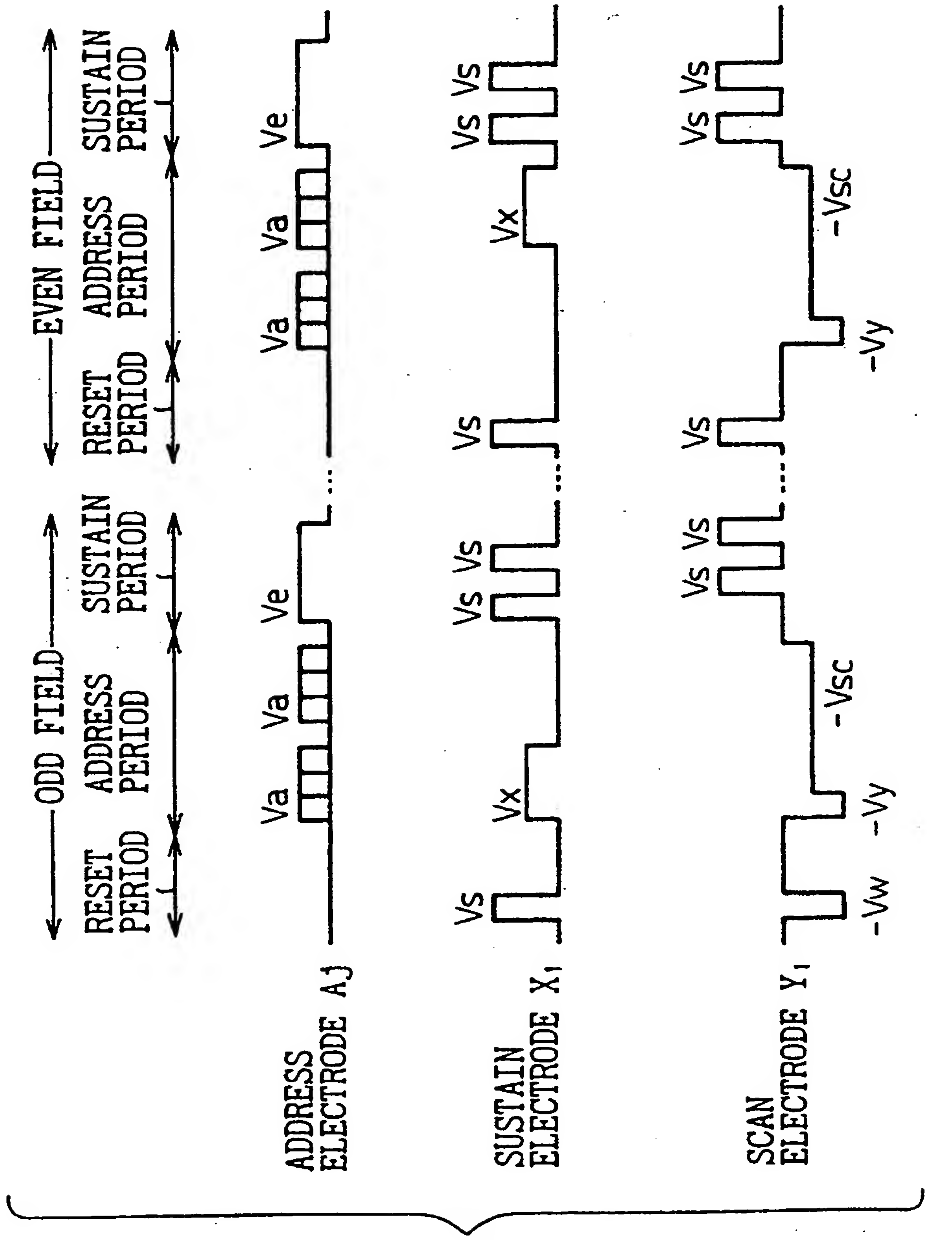

ODD FIELD
EVEN FIELD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
ADDRESS ELECTRODE Aj
SUSTAIN ELECTRODE X1
SCAN ELECTRODE Y1
Va
Ve
Vs
Vx
-Vw
-Vy
-Vsc

Fig.1a

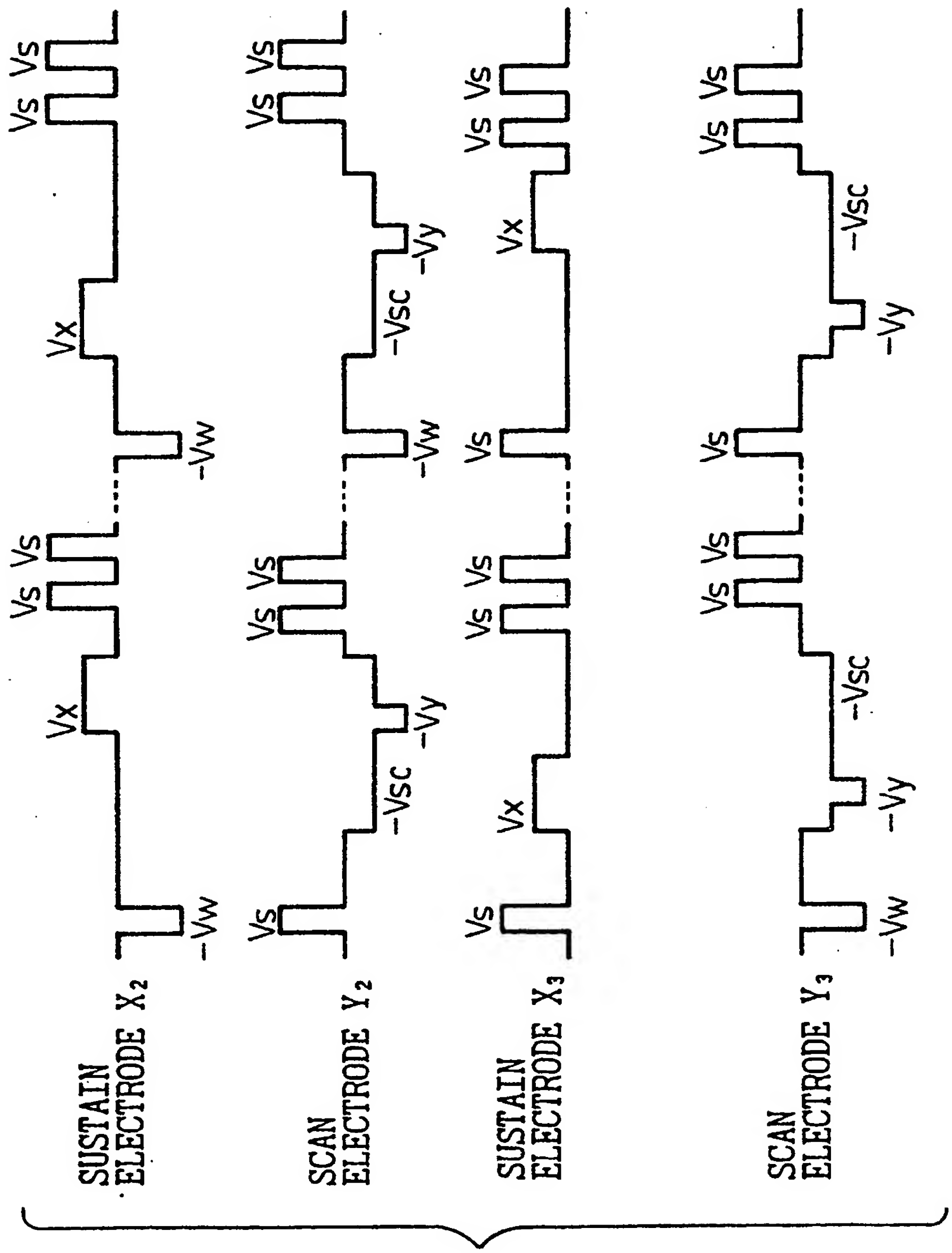

SUSTAIN ELECTRODE X_2
SCAN ELECTRODE Y_2
SUSTAIN ELECTRODE X_3
SCAN ELECTRODE Y_3
Vs
Vx
−Vw
−Vsc
−Vy

Fig.1b

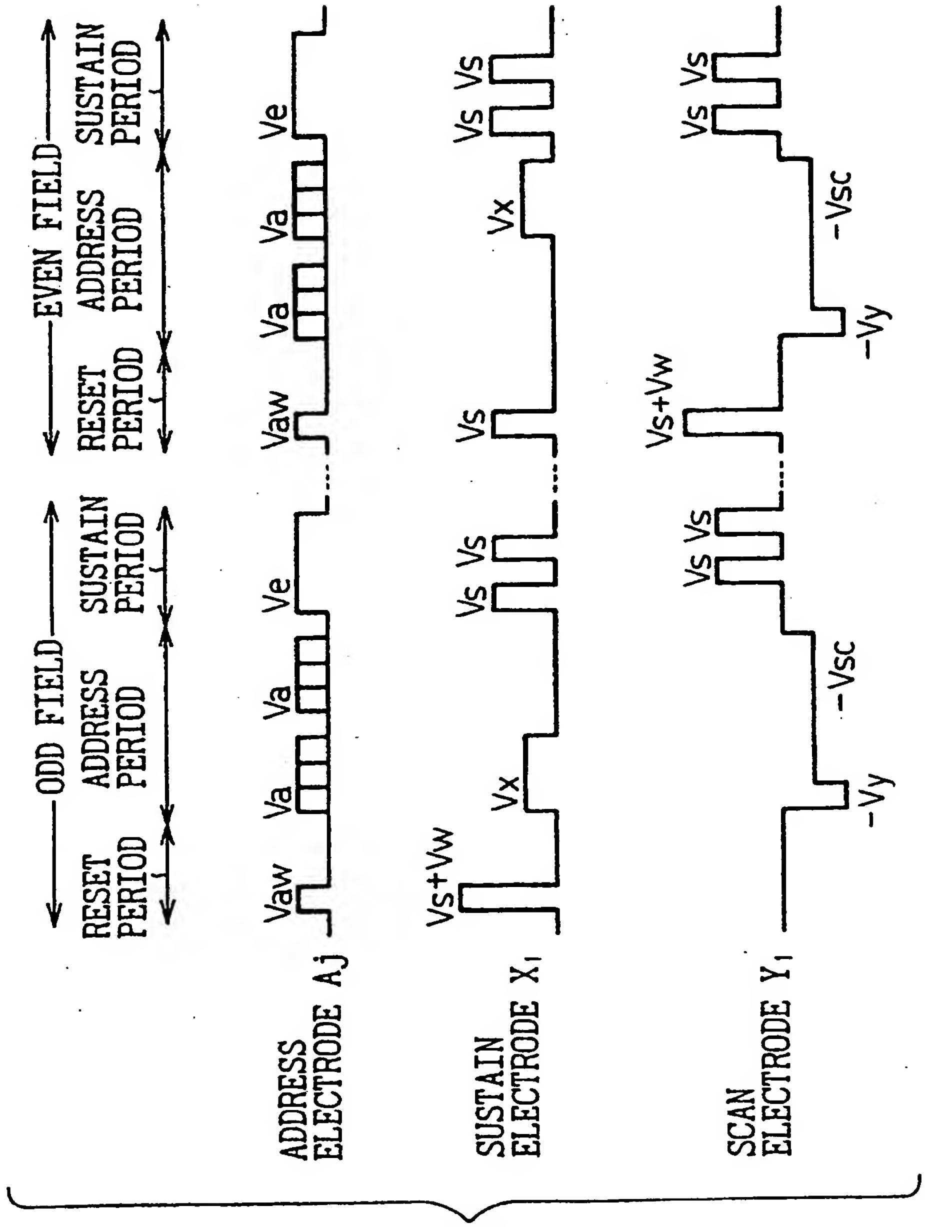

ODD FIELD
EVEN FIELD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
ADDRESS ELECTRODE Aj
SUSTAIN ELECTRODE X1
SCAN ELECTRODE Y1
Vaw
Va
Ve
Vs+Vw
Vx
Vs
-Vy
-Vsc

Fig.2a

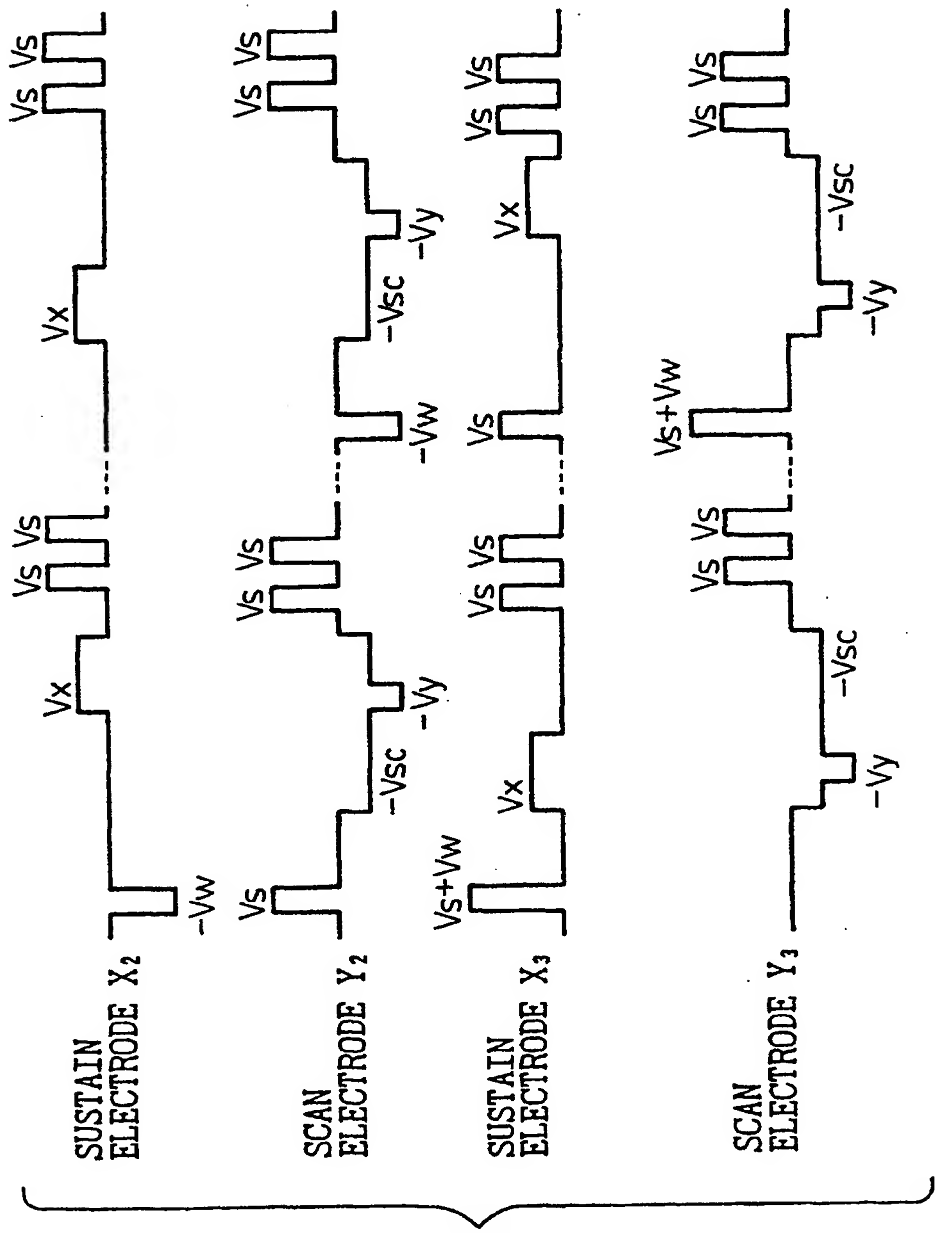

SUSTAIN ELECTRODE X₂
SCAN ELECTRODE Y₂
SUSTAIN ELECTRODE X₃
SCAN ELECTRODE Y₃
-Vw
Vs
Vs+Vw
Vx
Vs
-Vsc
-Vy
Vs+Vw

Fig.2b

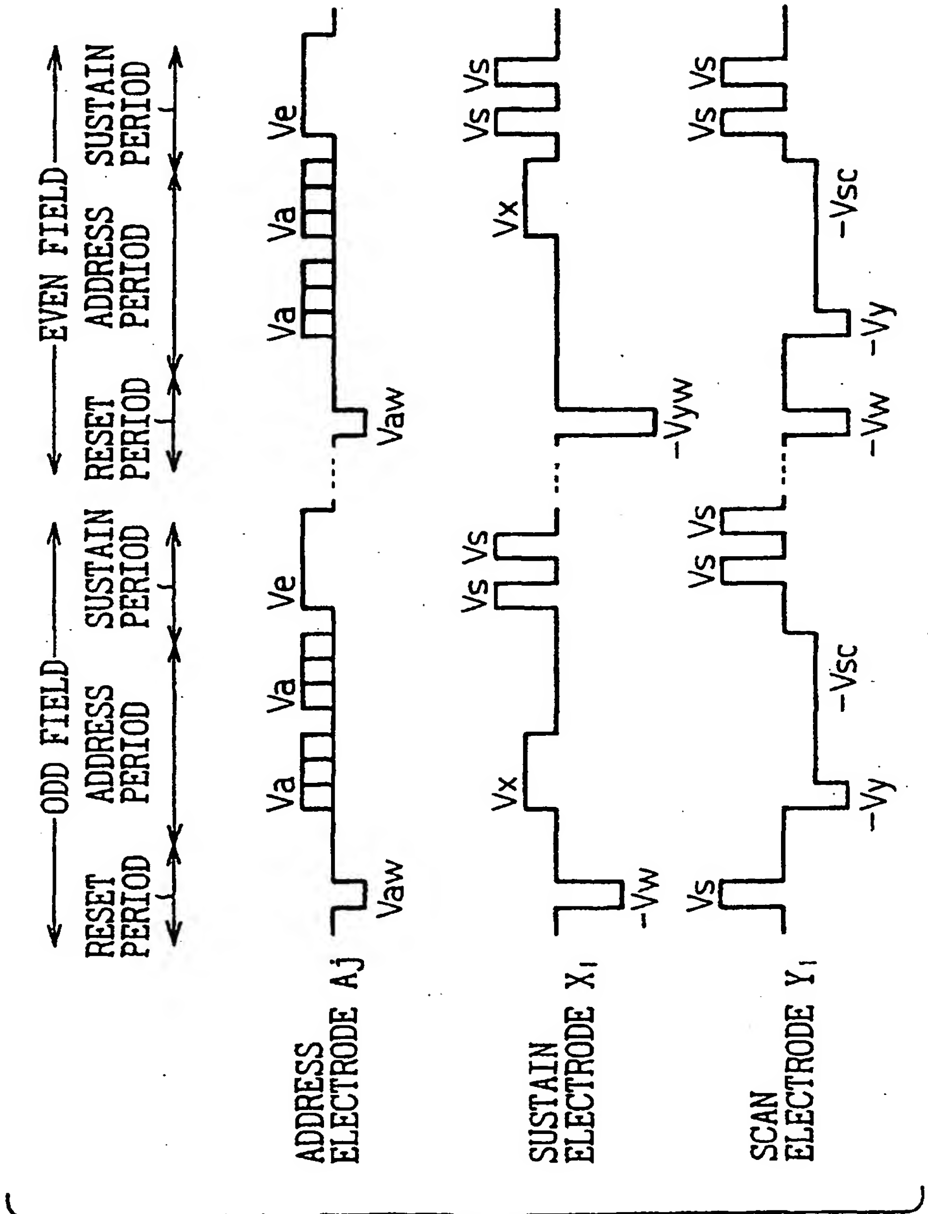

ODD FIELD
EVEN FIELD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
ADDRESS ELECTRODE Aj
SUSTAIN ELECTRODE X1
SCAN ELECTRODE Y1
Vaw
Va
Va
Ve
Vaw
Va
Va
Ve
-Vw
Vx
Vs
Vs
-Vyw
Vx
Vs
Vs
Vs
Vs
-Vy
-Vsc
Vs
Vs
-Vw
-Vy
-Vsc
Vs
Vs

Fig.3a

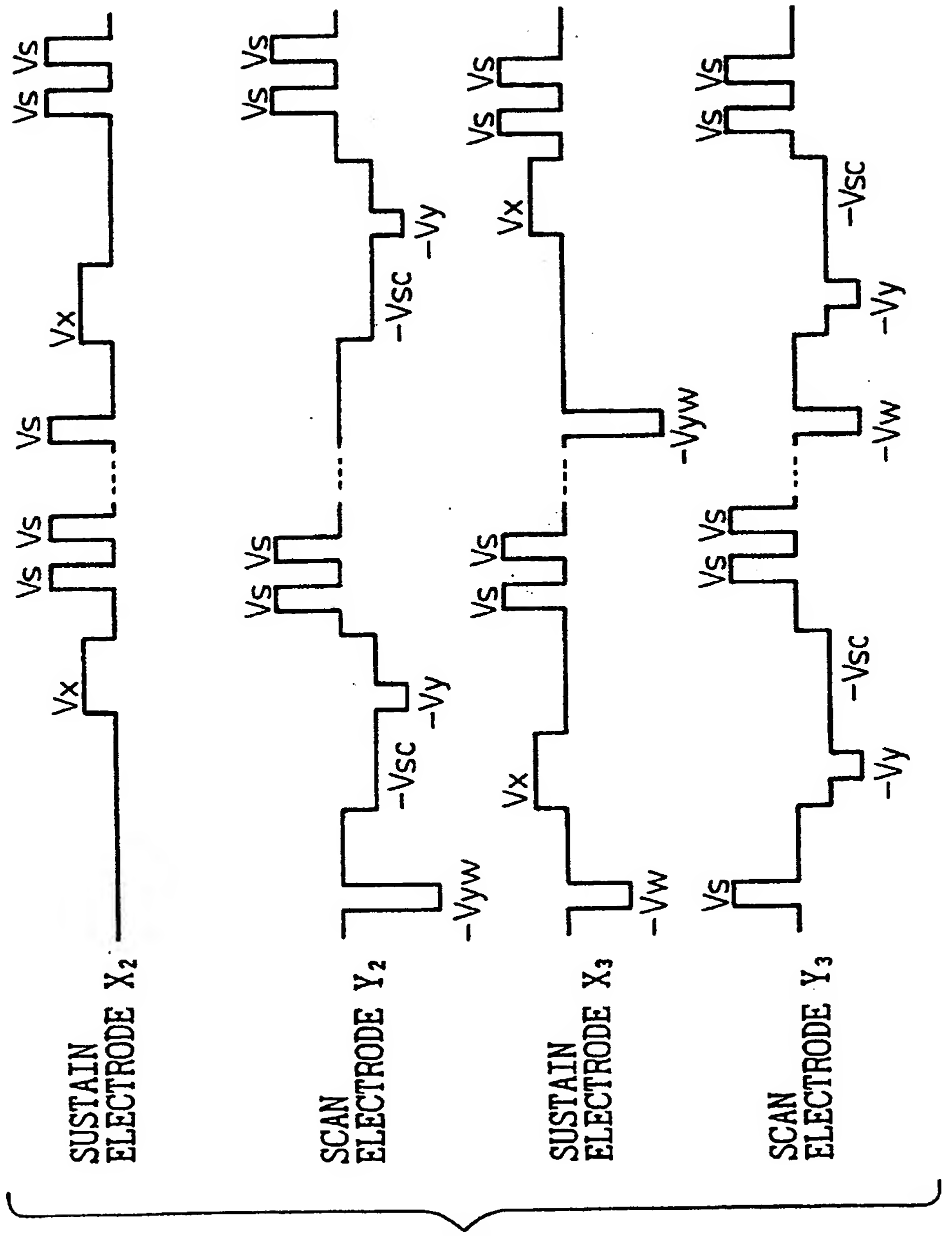

SUSTAIN ELECTRODE X2
SCAN ELECTRODE Y2
SUSTAIN ELECTRODE X3
SCAN ELECTRODE Y3
Vs
Vx
-Vyw
-Vsc
-Vy
-Vw

Fig.3b

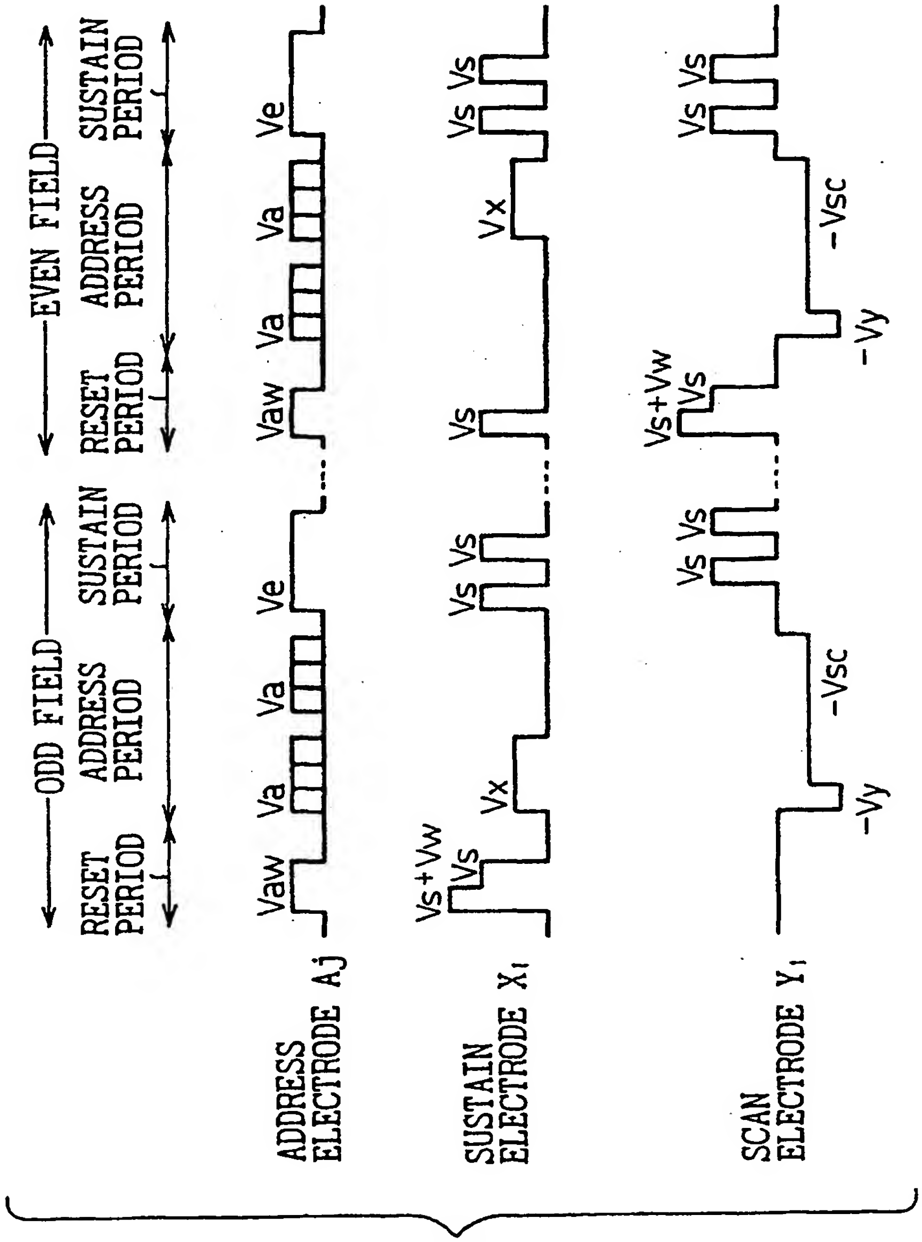

ODD FIELD
EVEN FIELD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
ADDRESS ELECTRODE Aj
SUSTAIN ELECTRODE X1
SCAN ELECTRODE Y1
Vaw
Va
Va
Ve
Vs+Vw
Vs
Vx
Vs
Vs
-Vy
-Vsc

Fig.4a

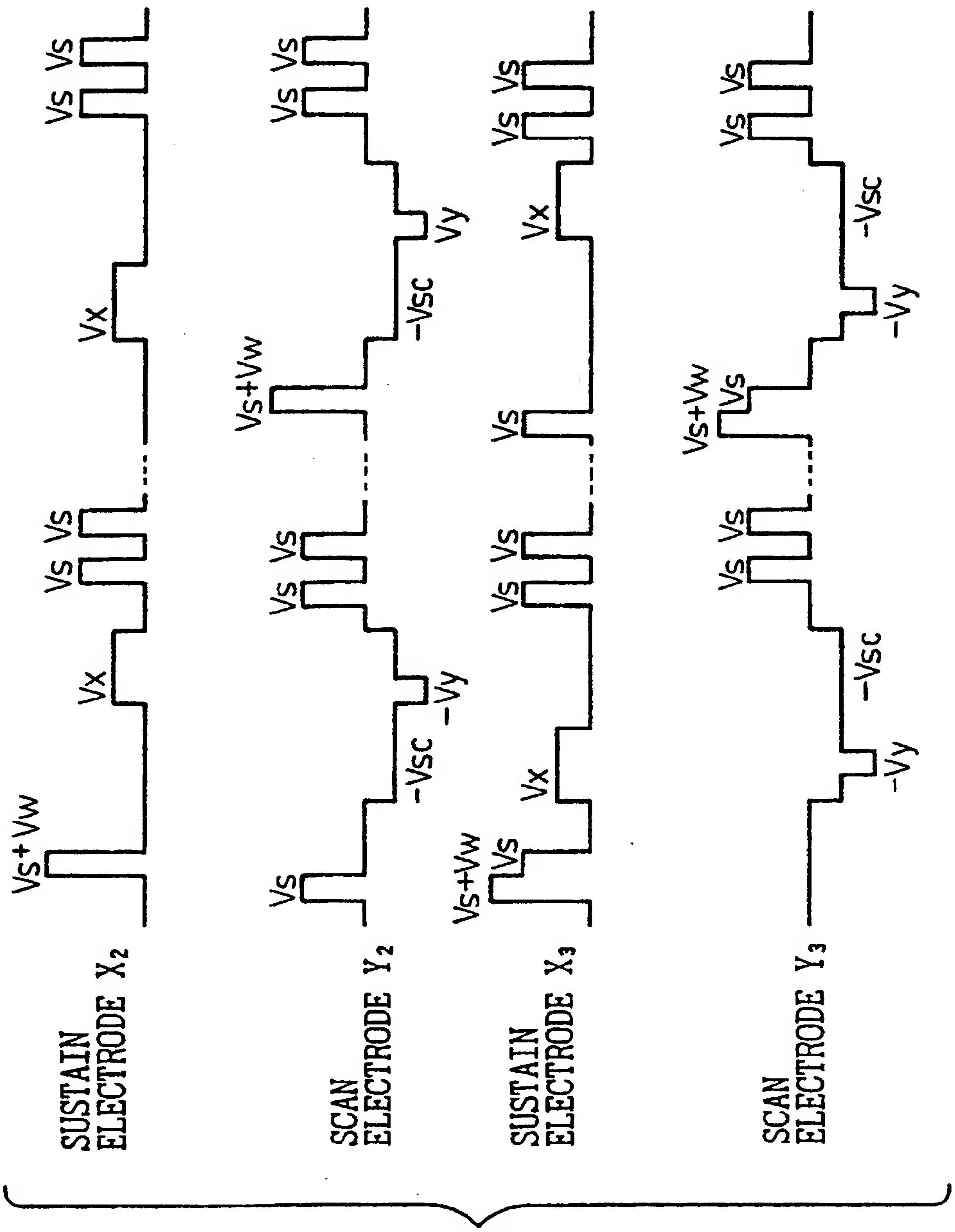

SUSTAIN ELECTRODE X_2
SCAN ELECTRODE Y_2
SUSTAIN ELECTRODE X_3
SCAN ELECTRODE Y_3
Vs+Vw
Vs
Vx
-Vsc
-Vy
Vy

Fig.4b

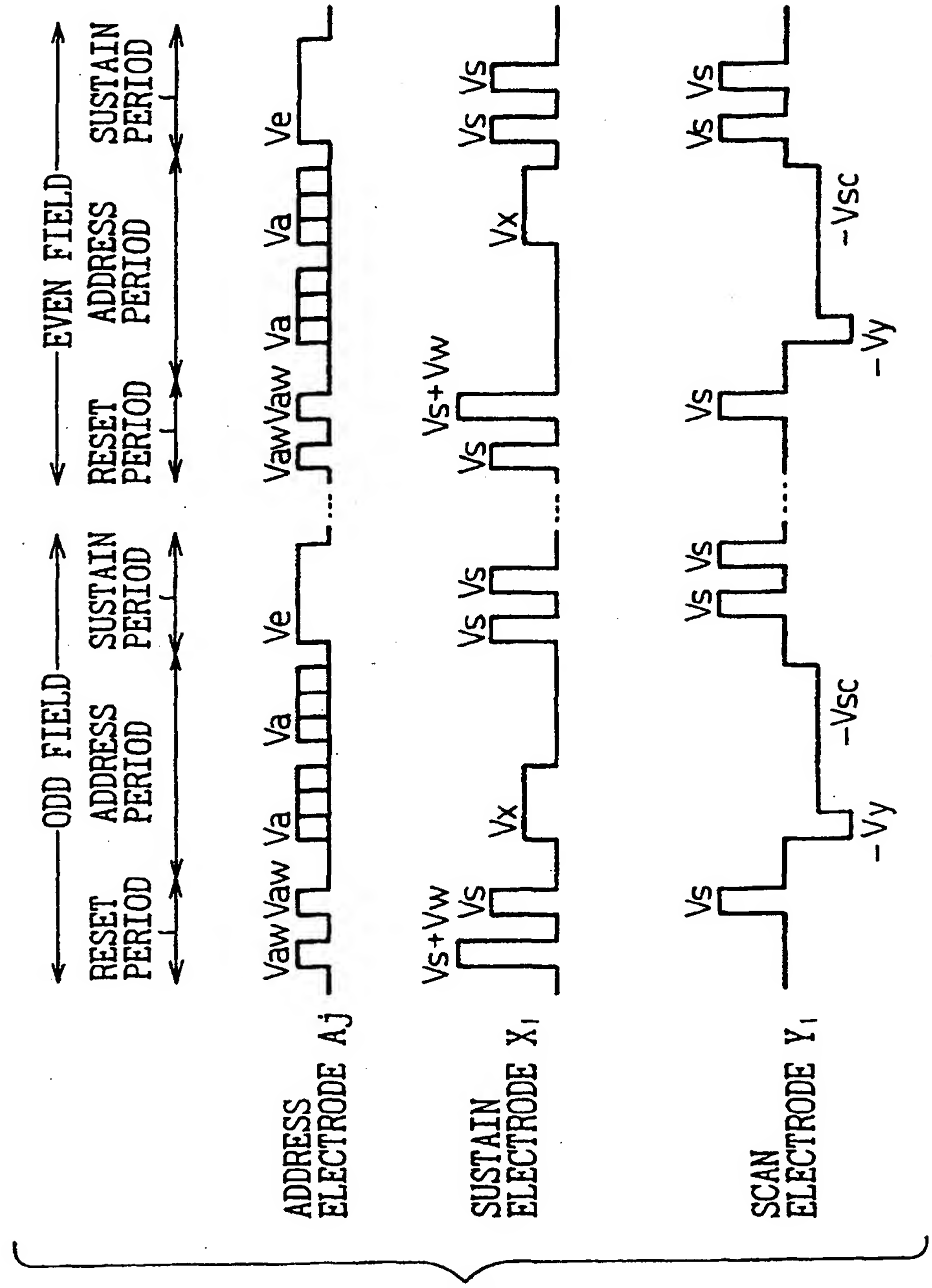

ODD FIELD
EVEN FIELD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
ADDRESS ELECTRODE Aj
SUSTAIN ELECTRODE X_1
SCAN ELECTRODE Y_1
Vaw Vaw Va Va Ve
Vs+Vw Vs Vx Vs Vs
Vs -Vy -Vsc Vs Vs

Fig.5a

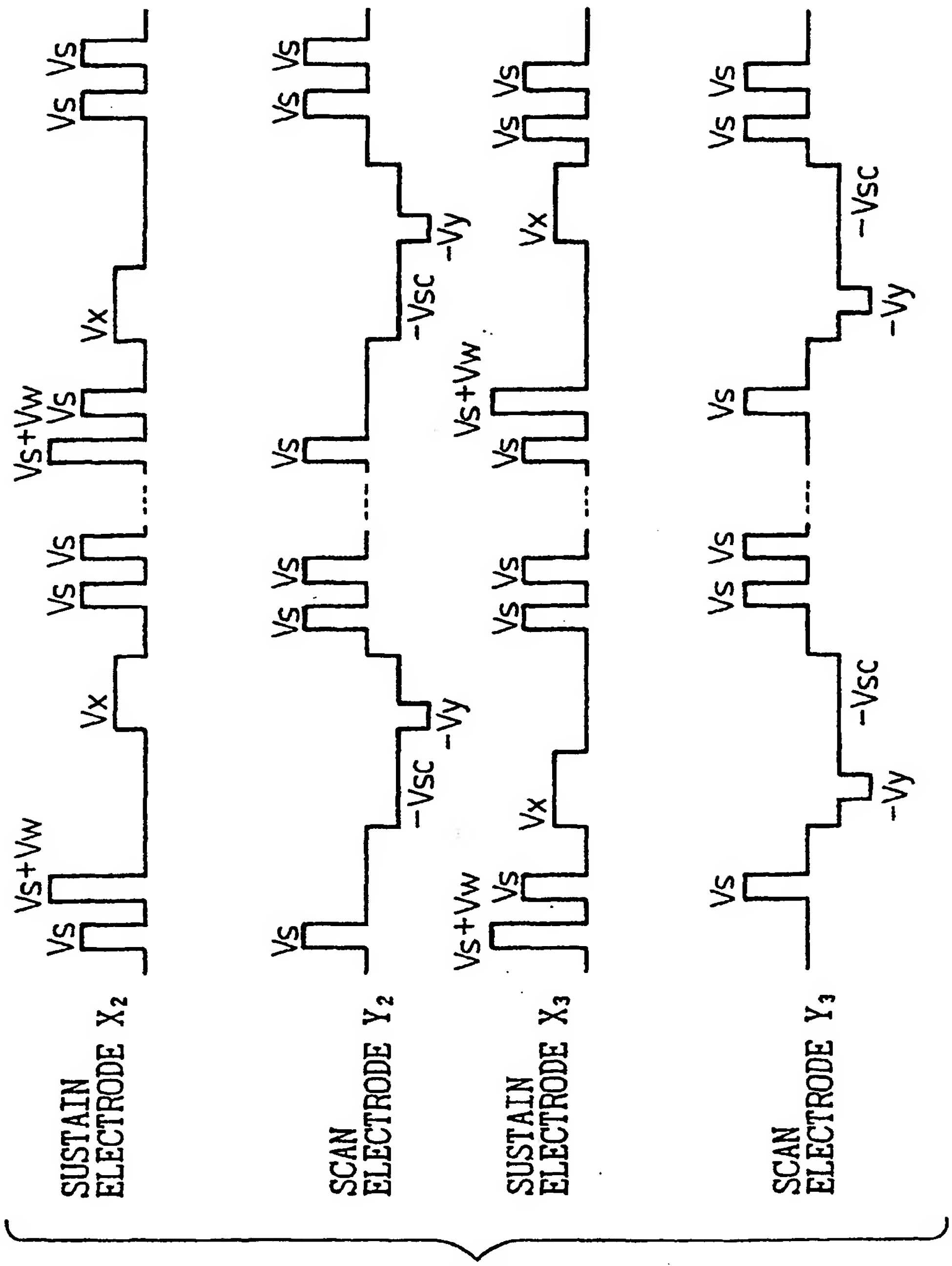
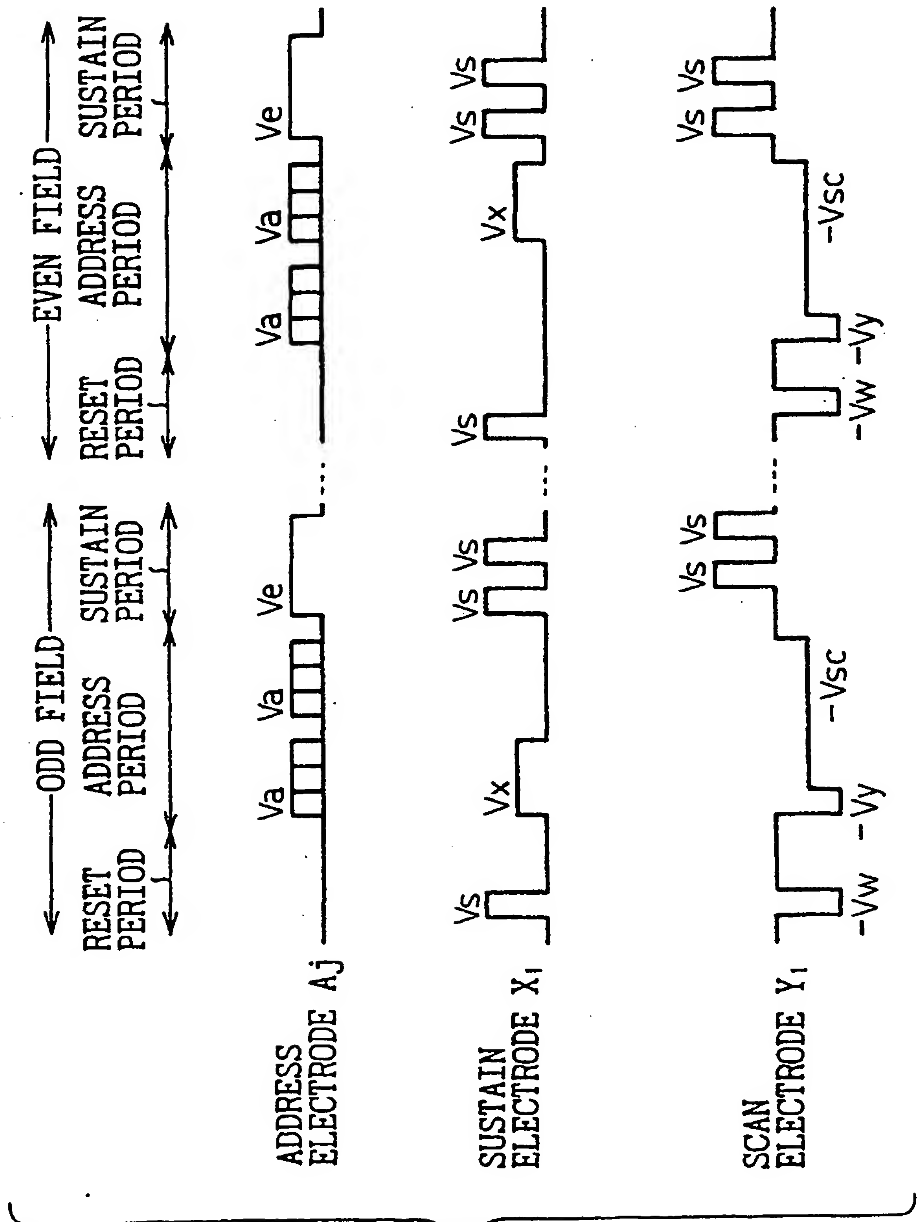
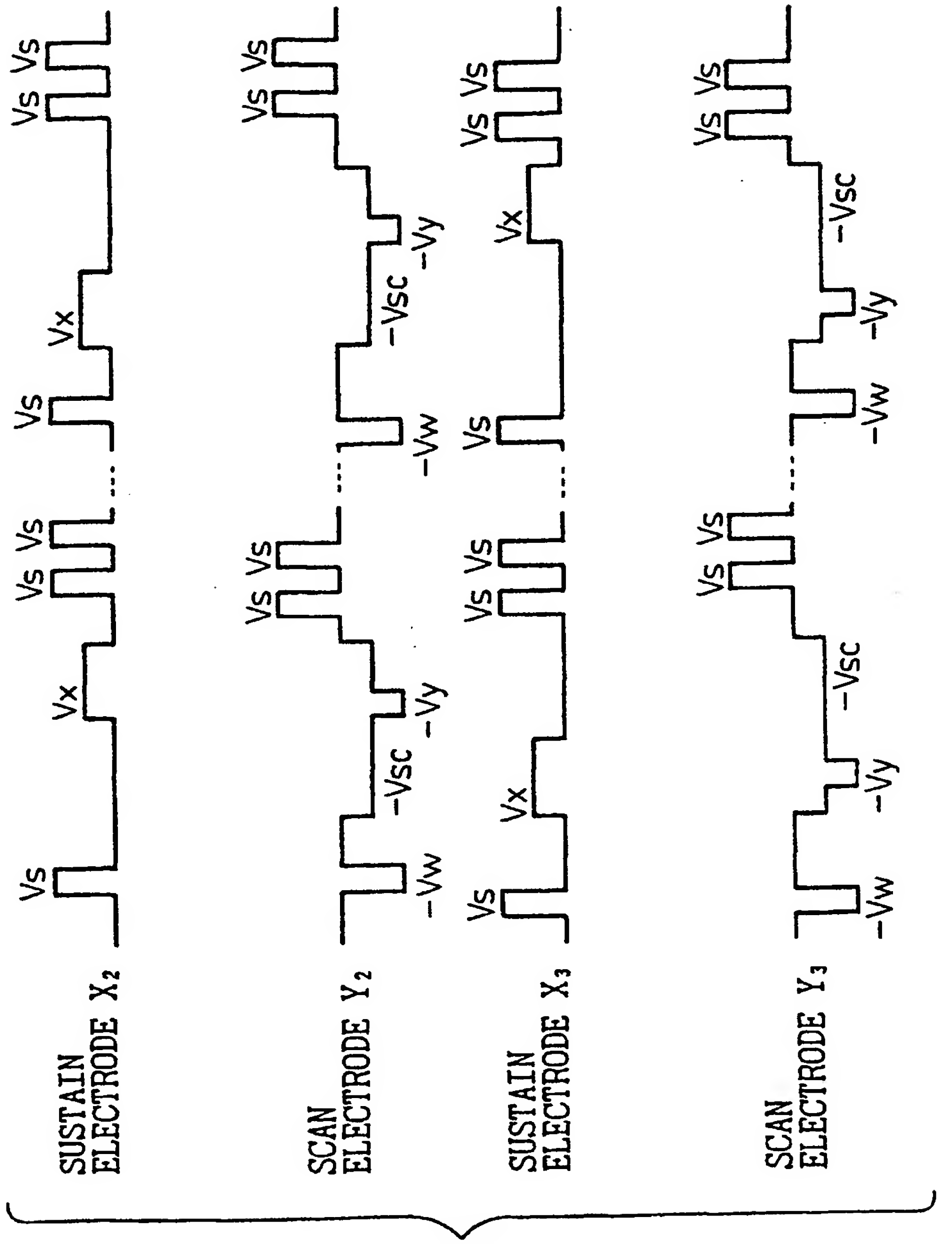

SUSTAIN ELECTRODE X2
SCAN ELECTRODE Y2
SUSTAIN ELECTRODE X3
SCAN ELECTRODE Y3
Vs
Vs+Vw
Vx
-Vsc
-Vy

Fig.5b



ODD FIELD
EVEN FIELD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
ADDRESS ELECTRODE Aj
Va Va Ve
Va Va Ve
SUSTAIN ELECTRODE X1
Vs Vx Vs Vs
Vs Vx Vs Vs
SCAN ELECTRODE Y1
-Vw -Vy -Vsc Vs Vs
-Vw -Vy -Vsc Vs Vs

Fig.6a



SUSTAIN ELECTRODE X_2
SCAN ELECTRODE Y_2
SUSTAIN ELECTRODE X_3
SCAN ELECTRODE Y_3
Vs
Vx
−Vsc
−Vy
−Vw

Fig.6b

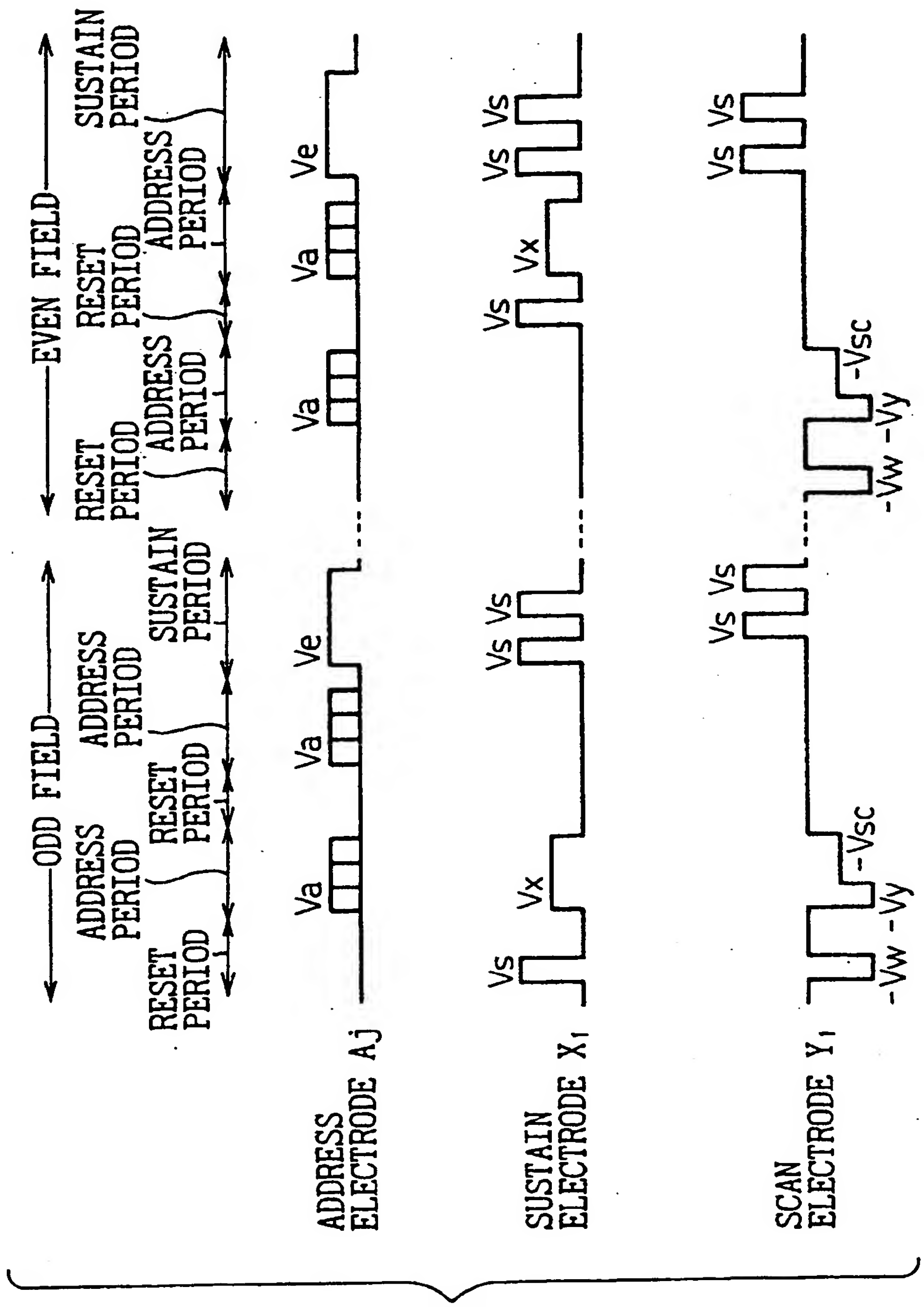

ODD FIELD
RESET PERIOD
ADDRESS PERIOD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
EVEN FIELD
RESET PERIOD
ADDRESS PERIOD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
ADDRESS ELECTRODE Aj
Va
Va
Ve
Va
Va
Ve
SUSTAIN ELECTRODE X1
Vs
Vx
Vs Vs
Vs
Vx
Vs Vs
SCAN ELECTRODE Y1
-Vw -Vy
-Vsc
Vs Vs
-Vw -Vy
-Vsc
Vs Vs

Fig.7a

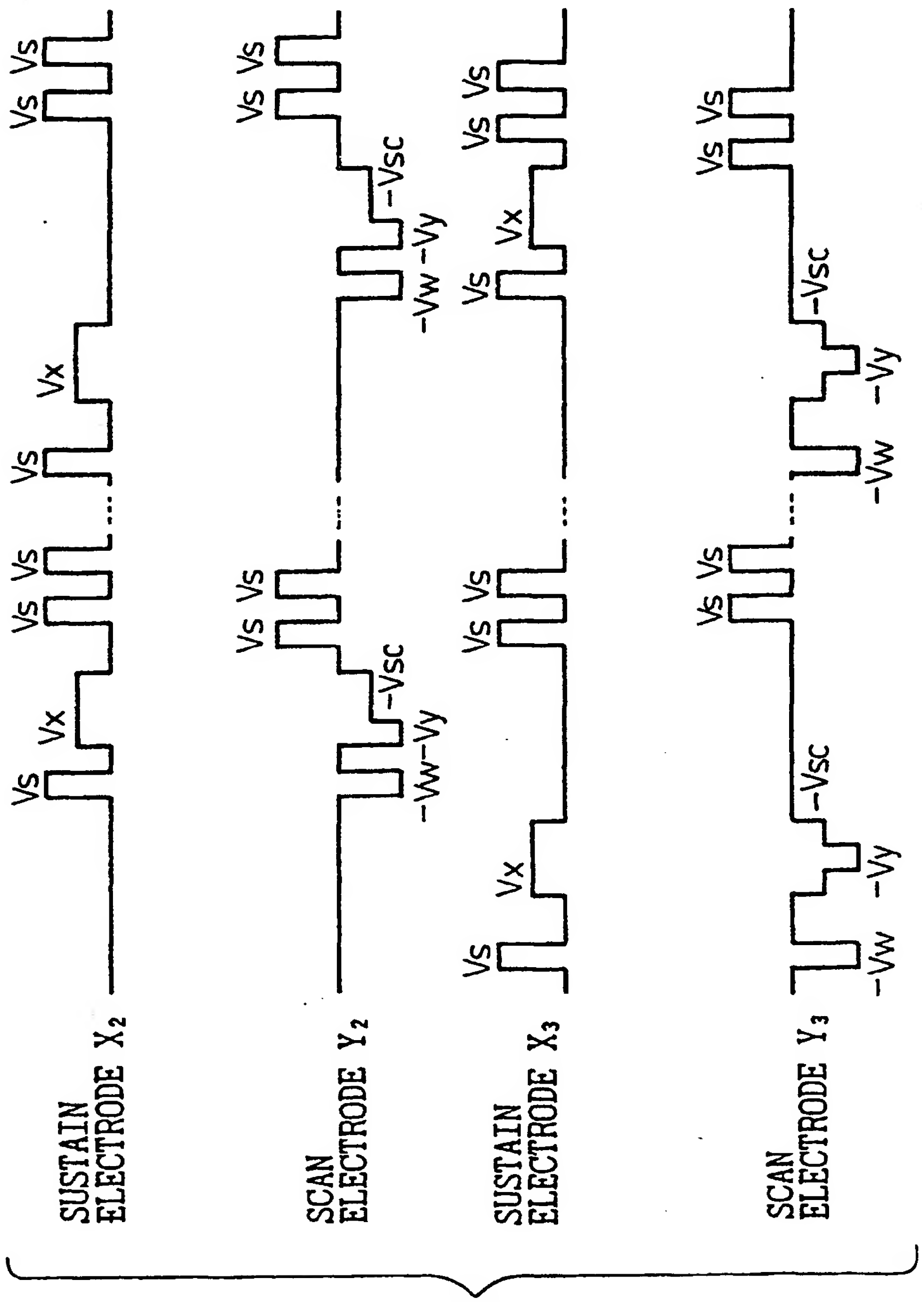

SUSTAIN ELECTRODE X_2
SCAN ELECTRODE Y_2
SUSTAIN ELECTRODE X_3
SCAN ELECTRODE Y_3
Vs
Vx
-Vsc
-Vw
-Vy

Fig.7b

Fig.8

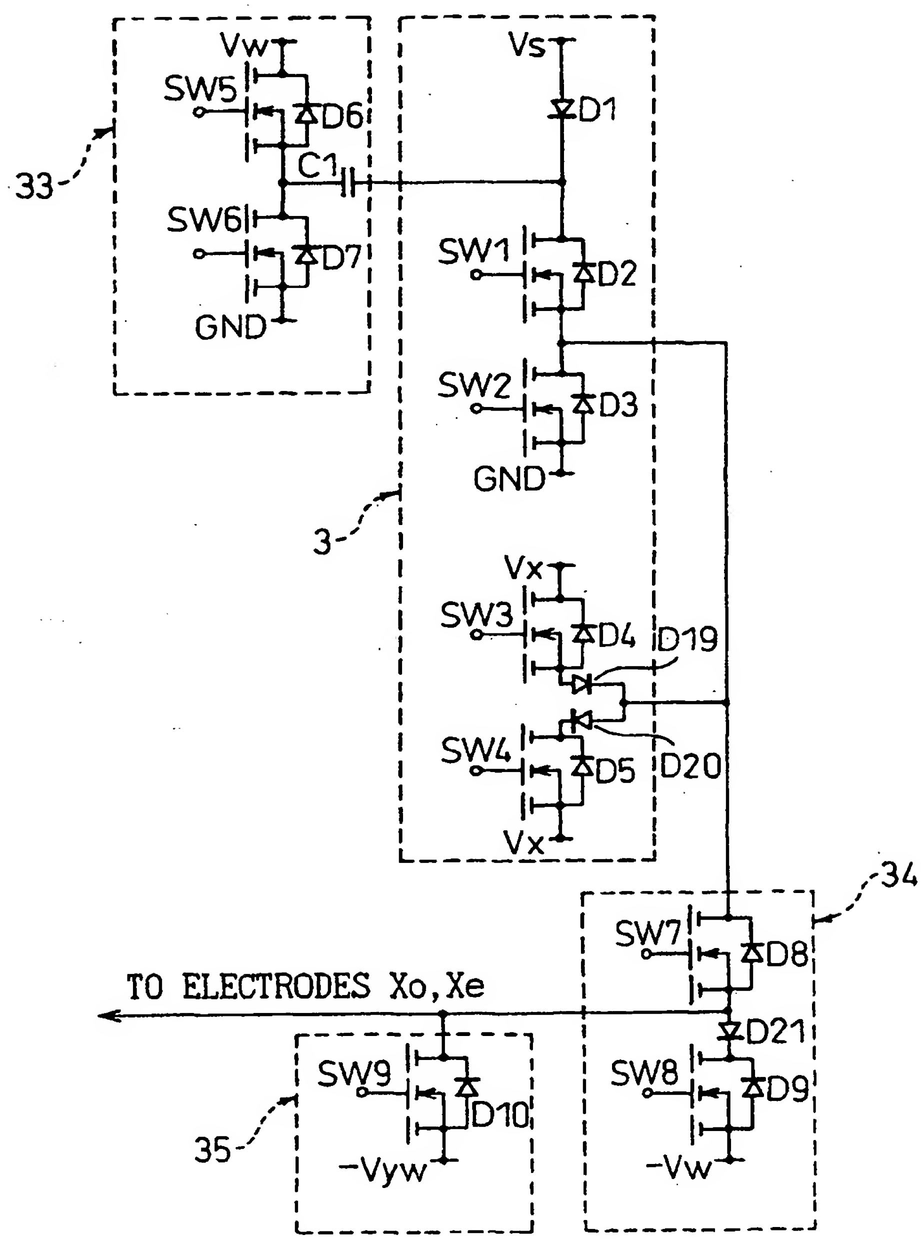

Vw
SW5
D6
C1
33
SW6
D7
GND
Vs
D1
SW1
D2
SW2
D3
GND
3
Vx
SW3
D4
D19
SW4
D5
D20
Vx
34
SW7
D8
TO ELECTRODES Xo,Xe
D21
SW9
D10
35
-Vyw
SW8
D9
-Vw

Fig.9

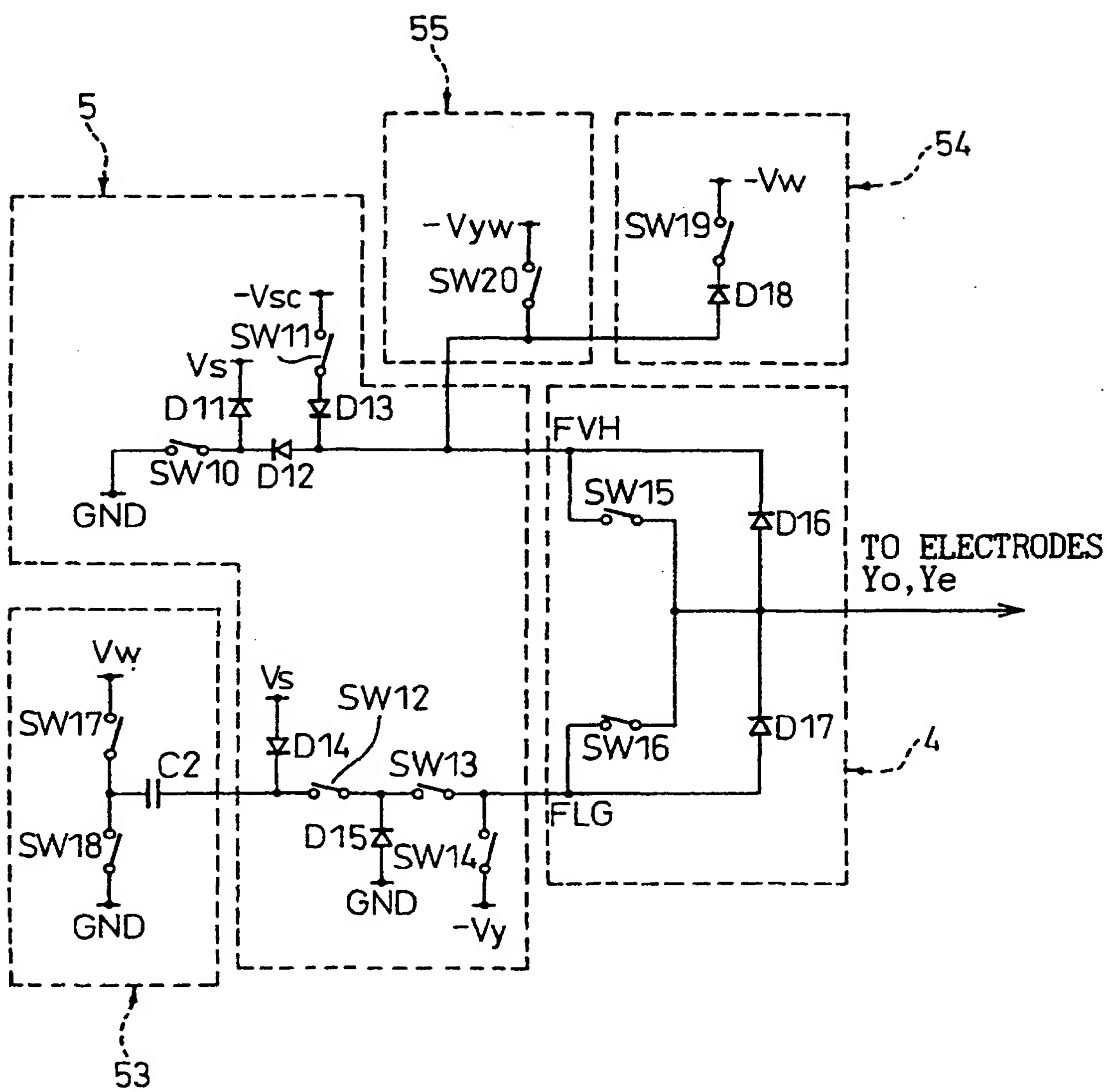

55
5
54
-Vyw
SW20
-Vw
SW19
D18
-Vsc
SW11
Vs
D11
D13
SW10
D12
GND
FVH
SW15
D16
TO ELECTRODES
Yo,Ye
Vw
SW17
C2
SW18
GND
Vs
D14
SW12
SW13
D15
SW14
GND
-Vy
SW16
D17
FLG
4
53

Fig.10

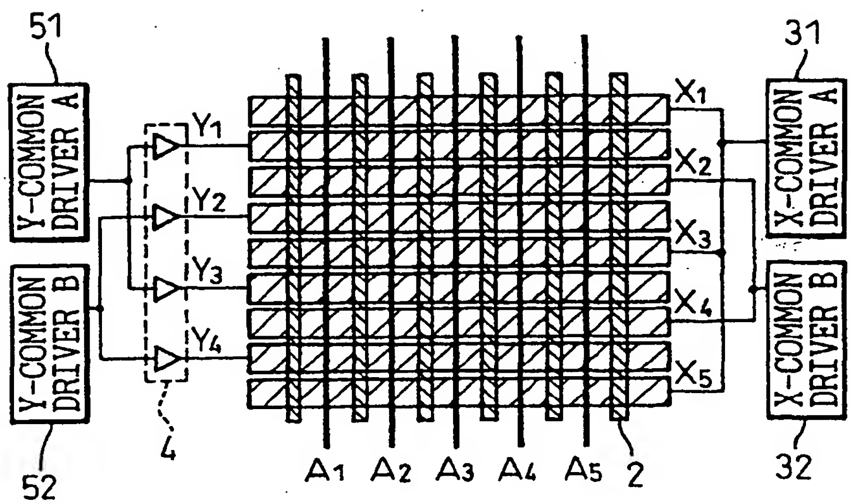

51
Y-COMMON DRIVER A
Y-COMMON DRIVER B
52
4
Y1
Y2
Y3
Y4
X1
X2
X3
X4
X5
A1 A2 A3 A4 A5 2
31
X-COMMON DRIVER A
X-COMMON DRIVER B
32

Fig.11

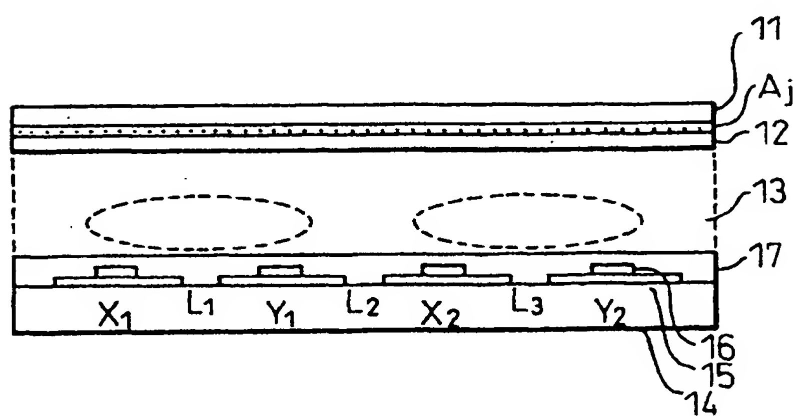
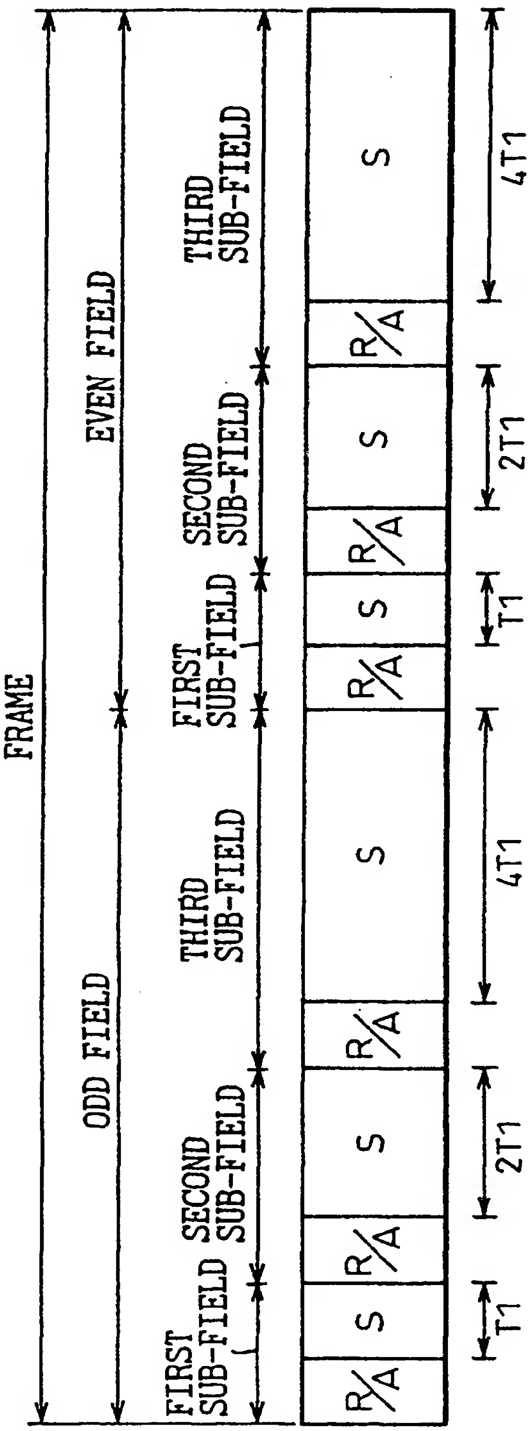

11
Aj
12
13
17
X1 L1 Y1 L2 X2 L3 Y2
16
15
14

Fig.12


FRAME
ODD FIELD
EVEN FIELD
FIRST SUB-FIELD
SECOND SUB-FIELD
THIRD SUB-FIELD
FIRST SUB-FIELD
SECOND SUB-FIELD
THIRD SUB-FIELD
R/A
S
R/A
S
R/A
S
R/A
S
R/A
S
R/A
S
T1
2T1
4T1
T1
2T1
4T1

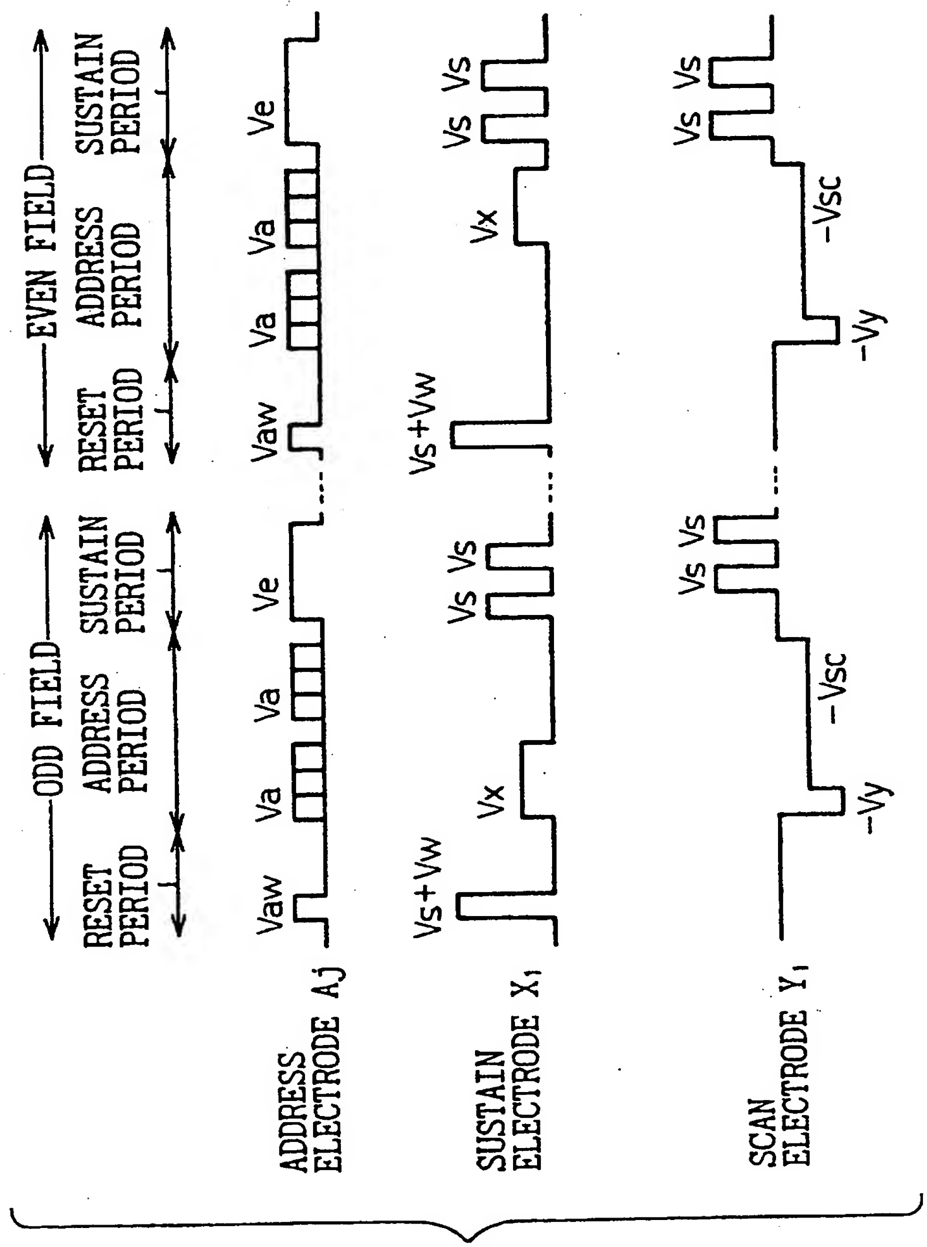

ODD FIELD
EVEN FIELD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
ADDRESS ELECTRODE Aj
Vaw
Va
Va
Ve
Vaw
Va
Va
Ve
SUSTAIN ELECTRODE X1
Vs+Vw
Vx
Vs
Vs
Vs+Vw
Vx
Vs
Vs
SCAN ELECTRODE Y1
-Vy
-Vsc
Vs
Vs
-Vy
-Vsc
Vs
Vs

Fig.13a

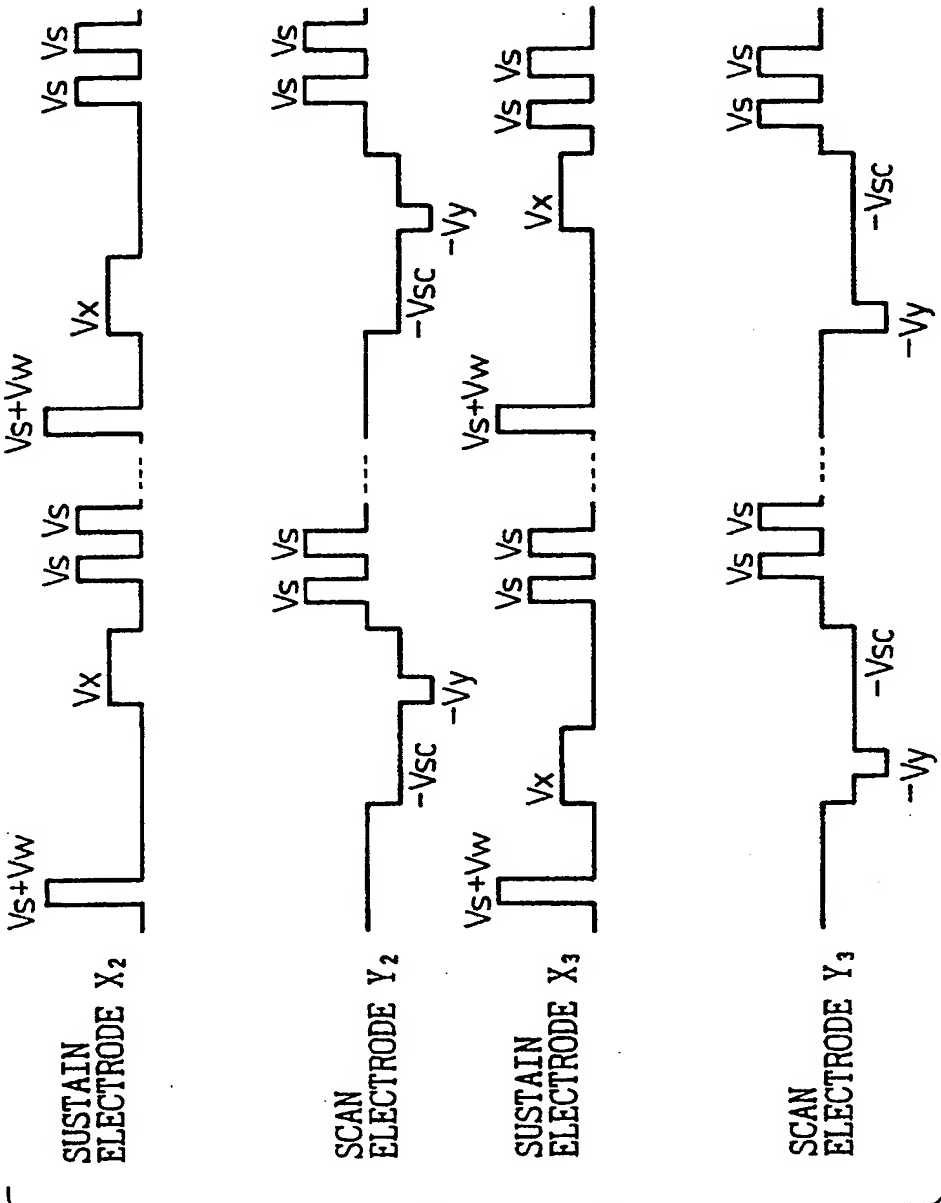

SUSTAIN ELECTRODE X_2
SCAN ELECTRODE Y_2
SUSTAIN ELECTRODE X_3
SCAN ELECTRODE Y_3
Vs+Vw
Vx
Vs
Vs
Vs+Vw
Vx
Vs
Vs
-Vsc
-Vy
Vs
Vs
-Vsc
-Vy
Vs
Vs
Vs+Vw
Vx
Vs
Vs
Vs+Vw
Vx
Vs
Vs
-Vy
-Vsc
Vs
Vs
-Vy
-Vsc
Vs
Vs

Fig.13b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 30 6454

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 436 634 A (KANAZAWA) * abstract * * column 4, line 15 - line 37 * * column 8, line 31 - line 51 * * column 9, line 36 - line 52; figures 11-13 * ---	1-30	G09G3/28
A	PATENT ABSTRACTS OF JAPAN vol. 17, no. 257 (E-1368), 20 May 1993 & JP 05 002993 A (FUJITSU LTD.), 8 January 1993, * abstract * ---	1-30	
A	PATENT ABSTRACTS OF JAPAN vol. 14, no. 520 (E-1022), 14 November 1990 & JP 02 220330 A (FUJITSU LTD.), 3 September 1990, * abstract * ---	1-30	
P,A,D	EP 0 762 373 A (FUJITSU LTD.) * abstract; figure 4 * ---	1-30	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G09G
A	US 5 029 257 A (KIM) * abstract * * column 2, line 58 - line 65 * * column 4, line 32 - line 39; claim 2; figures 2,4,5 * -----		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 November 1997	O'Reilly, D

CATEGORY OF CITED DOCUMENTS

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